AMPEX

AMPEX
MCM-8086
CORE MEMORY MODULE
TECHNICAL MANUAL

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AMPEX MEMORY PRODUCTS DIVISION

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Ampex Corporation, Memory Products Division
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SECTION I
GENERAL DESCRIPTION

1.1 SCOPE OF MANUAL

This manual contains installation, operation, and maintenance instructions for the MCM-8086 Microcomputer Core Memory module manufactured by Ampex Corporation, Memory Products Division, El Segundo, California.

1.2 GENERAL DESCRIPTION

The MCM-8086 Microcomputer Core Memory module, shown in Figure 1-1, replaces or expands the memory for Intel Multibus-based† microprocessors. An all-electronic random access data storage unit, the MCM-8086 uses ferrite cores as the storage element. The MCM-8086 has a storage capacity of 32,768 words of 16 bits. Four byte transfer operations are possible. Each module is a complete memory system with its own address and data register, timing and control logic interface; and decode, drive, and sense circuits. The memory module performs read-restore and clear-write memory operations.

1.3 EQUIPMENT CHARACTERISTICS

Physical, electrical, and mechanical characteristics are listed in Table 1-1.

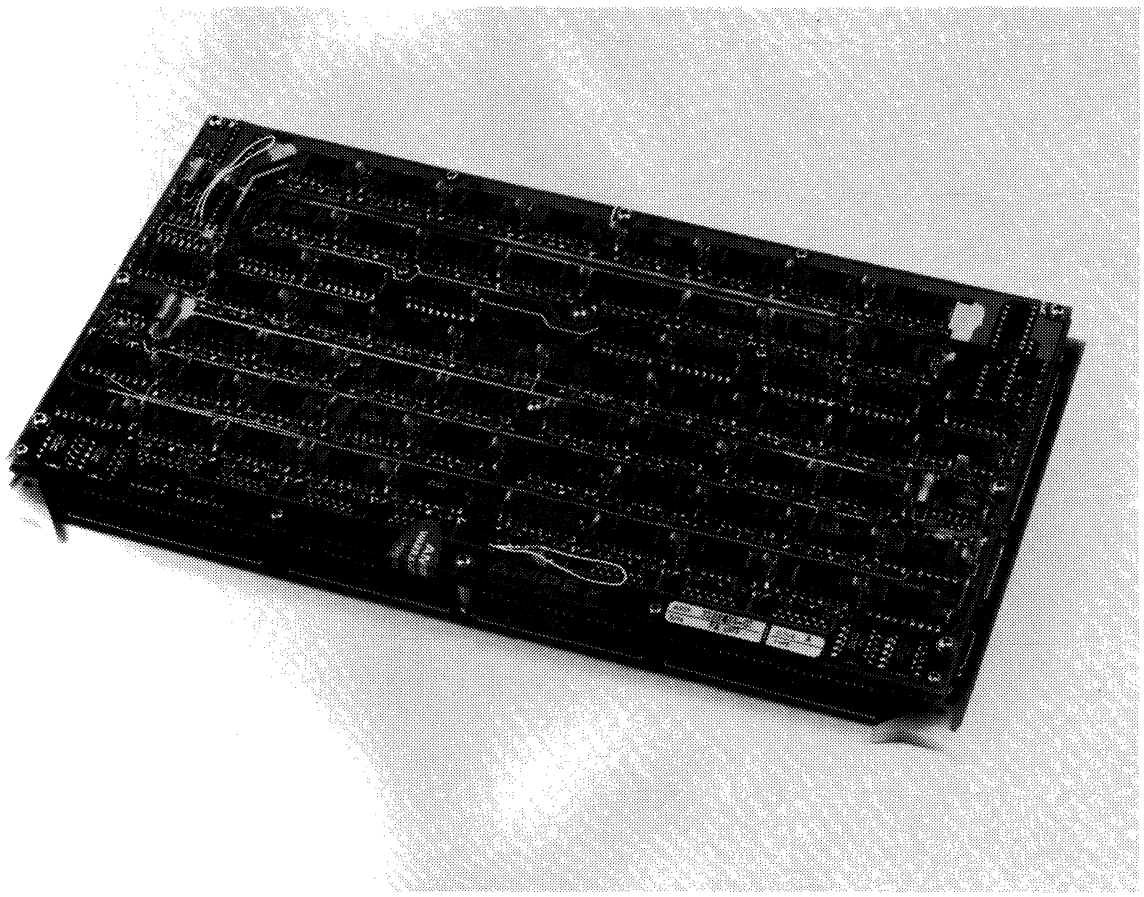


Figure 1-1. MCM-8086 Microcomputer Core Memory Module

† Multibus is a registered trademark of Intel Corporation.

Table 1-1. Specifications

Parameter	Characteristic
Equipment	
Identification	Ampex MCM-8086
Type	Magnetic Core Memory
Mounting	Plug-in PWB connectors in card cage
Width	6.75 inches (171.45 mm)
Length	12.00 inches (304.80 mm)
Thickness*	1.135 inches (28.83 mm)
Power Requirements	
Supply Voltages	+5 VDC ±5% +12 VDC ±5%
Load	Condition +5 VDC +12 VDC Standby 3.1A 0.9A All "0" 4.3A 3.3A WP** 3.7A 2.6A
Storage Capacity	32,768 words (65,536 Bytes)
Word Length	16 bits
Cycle Time	Read/Restore: 900 nanoseconds Clear/Write: 1000 nanoseconds (delayed write) Clear/Write 1500 nanoseconds (advance write)
Addressing	Random access
Address Select Expansion	1 megabyte with 16K byte boundary

* Takes up 2 slots in Intel chassis

** WP (Worst Pattern): 50% "zeros" and 50% "ones"

Table 1-1. Specifications (contd.)

Parameter	Characteristic
Operating Modes	Read-Restore Clear-Write Byte Control, Access Inhibit, Write Protect } Special Features
Data Save	No data loss upon power failure
Decoding	ACD (Ampex Core Driver)
Core Selection	3-wire, 3-dimensional
Interface	TTL negative True logic
Logic Levels	
False (high)	2.0 volts to 5.5 volts
True (low)	0.0 volts to 0.8 volts
Rise and Fall Times (max)	50 nanoseconds, (10% to 90%)
Temperature	
Operating	0^{o} to $55^{o}C$
Nonoperating	$-55^{o}C$ to $85^{o}C$
Humidity	Up to 95%, without condensation
Cooling Requirements	Airflow of 23 CFM through module along the 12" axis
Bus	Intel Multibus

SECTION II
INSTALLATION AND OPERATION

2.1 GENERAL

This section contains unpacking, installation, and operating instructions for the Ampex MCM-8086 Microcomputer Core Memory module.

2.2 RECEIVING INSPECTION

The memory modules are fully assembled and operationally checked prior to shipment from the factory. The units are individually packed in accordance with standard practices for electronic instrumentation equipment, and every precaution is taken to ensure that each system leaving the factory is complete and ready for installation. It is recommended, however that before they are opened, the containers should be inspected for evidence of damage and the number of packages be checked against the shipping list.

The carrier and the manufacturer should be notified of the nature and extent of any damage. Open the shipping container and remove the contents only if there is no shipping damage. Check the items removed from the container against the shipping list to verify the contents. Notify Ampex immediately if there is an apparent packing shortage.

2.3 MEMORY MODULE INSTALLATION

The memory module, as illustrated in Figure 2-1, is a 6.75 by 1.135 by 12.00 inch unit designed to plug into a card cage with 0.60 inch connector spacing. Each MCM-8086 memory module occupies two slots in a multibus card cage. The following paragraphs, figures, and tables provide detailed information to aid in the installation and operation of the module.

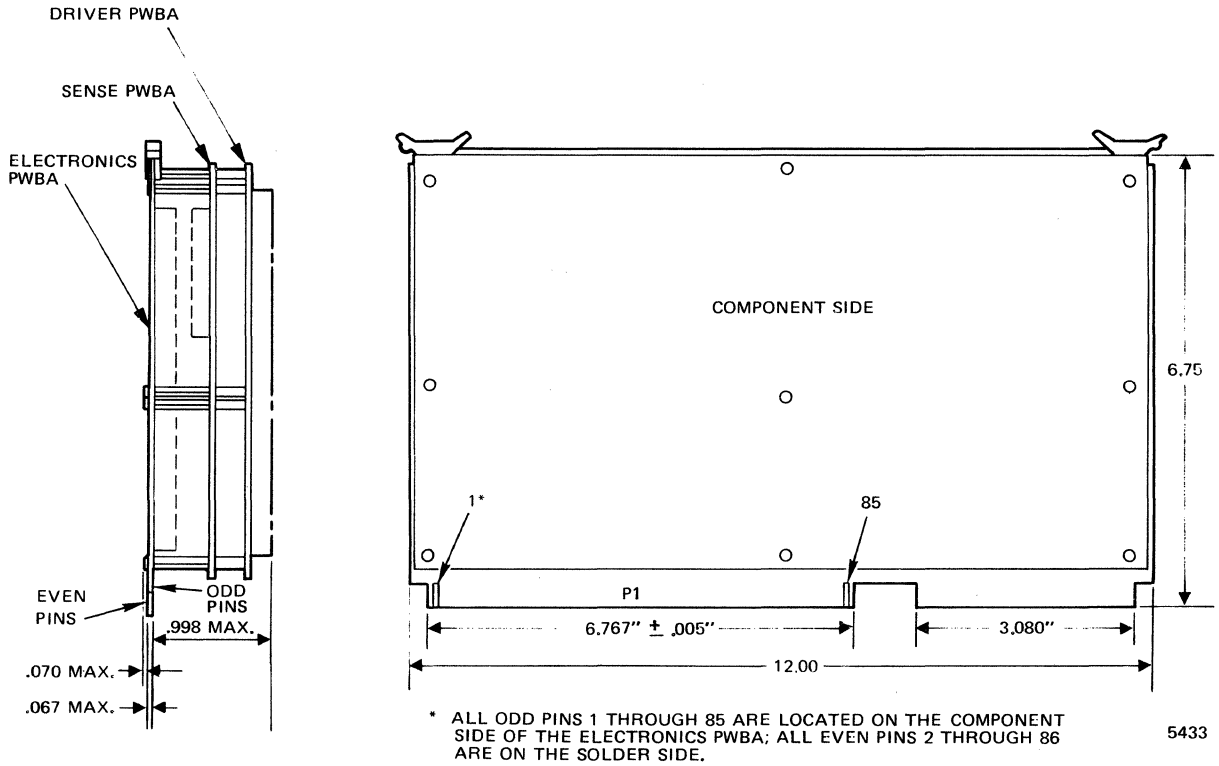


Figure 2-1. Memory Module Dimensions

2.3.1 Power Requirements

Power requirements for the memory module are specified in Table 1-1. Voltage tolerances include line, load, ripple, and temperature variations. No temperature compensation or on/off sequencing is required.

2.3.2 Cooling Requirements

An airflow of 23 cubic feet per minute (CFM) through the 12 inch axis of the module is required for cooling purposes. Ambient air temperature should not exceed +55°C at any time after dc power is applied.

2.3.3 Input/Output Signals

All input signals to the memory terminate in TTL integrated circuits. Input signals are all single-rail, and the complement of the signals is not required.

A true or low logic level digital input signal has voltage of less than +0.8 volts. A false or high logic level input signal has voltage more positive than +2.0 volts. Timing relationships are defined and measured from V_{REF}, which equals 1.5V for Schottky and 1.3V for low power Schottky devices. Both "LS" and "S" devices are used for address and control lines.

All data output signals are driven from TTL integrated circuit tristate drivers that are capable of sinking 40 Ma while maintaining a true (low) logic level from 0.0 to +0.5 volts. A false (high) signal has a voltage more positive than +2.4 volts. Input currents on the bi-directional data lines are less than –40 Ma at input level of 0.4V. The tristate data output permits parallel expansion of the memory by simply plugging in additional modules.

For a description of input and output signals, refer to Table 2-1.

2.3.4 I/O Connectors

Input/output signals and power connections to and from the memory module are made through connector P1 (see Figure 2-1), which is an 86-contact, double-sided, printed-circuit connector for 0.062 inch thick boards with 0.156 inch spacing. Connector P2 is not used for memory interface connection. The mating connector for P1 is Control Data type VPB01E43A00A1 or equivalent.

Table 2-2 lists the pin assignments for memory interface connector P1.

2.3.5 Data Save

The memory module is designed to prevent loss of data during power-on and power-off. An internal comparator circuit monitors the +5V and +12V sources to generate PSOK (Power Supply Okay). PSOK goes true (low) when both +5V and +12V are outside of safe limit. When PSOK goes low, the module will not accept any new memory cycles and is held reset until +5V and +12V rise to a safe level.

2.3.6 Module Select Switches

The memory module select address is determined by DIP switch SW2, (see Figure 2-2). Tables 2-3 and 2-4 provide the information to configure the memory module. Table 2-3 lists addresses on 64K byte boundaries; Table 2-4 lists addresses on 16K byte boundaries.

2.3.7 Write Protect and Access Inhibit

The memory module provides Write Protect or Access Inhibit options. Only one option can be utilized at any time. During Write Protect, the protected address block can be accessed only during a Read/Restore cycle. The protected block, of the memory, therefore, acts like a ROM. During Access Inhibit, the protected address block cannot be accessed at all. This is useful if another peripheral has address blocks overlapping with the memory.

The size of the protected address block is selected in both options with SW1-1 through SW1-4 (refer to Table 2-5). The block size can be incremented by 4K bytes and is additive from the starting address. For example: assume starting address is 32K bytes. SW1-4 is off and SW 1-3 through SW1-1 is on; with this condition, 60K bytes of memory can be protected. On the system level the address block protected lines between 32K bytes and 92K bytes.

The Write Protect and Access Inhibit is selected by SW1-5 and SW1-6 as listed in Table 2-5.

Table 2-1. Input/Output Signals

<table>
<tr><th>Signal</th><th>No. of Lines</th><th>Description</th></tr>
<tr><td>Initialize (INIT/)</td><td>1</td><td>INIT/ is a negative-true input signal that resets and initializes memory module registers and timing circuits.</td></tr>
<tr><td>Memory Read Command (MRDC/)</td><td>1</td><td>MRDC/ is a negative-true input signal that initiates a read-restore memory cycle. The address lines must be stable at least 50 nanoseconds prior to assertion of MRDC/. MRDC/ can be removed after the memory module asserts XACK/.</td></tr>
<tr><td>Memory Write Command (MWTC/)</td><td>1</td><td>MWTC/ is a negative-true input signal that initiates a clear-write memory cycle. The address lines and data bus must be stable at least 50 nanoseconds prior to assertion of MWTC/. MWTC/ may be removed after the memory module outputs XACK/.</td></tr>
<tr><td>Address (ADR0/ – ARD13/)</td><td>20</td><td>ADR0/ through ADD9/, ADRA/ through ADRF/, and ADR10/ through ADR13/ are 20 negative-true input signals that specify the memory module location to be written or read. ADR0/ through ADR13/ must be stable at least 50 nanoseconds prior to assertion of MWTC/ or MRDC/, and must remain stable until 50 nanoseconds after MWTC/ or MRDC/ is removed. The functions of ADR0/ through ADR13/ are listed below.
<table>
<tr><th>Address Line</th><th>Function</th></tr>
<tr><td>ADR0/ (LSB)</td><td>ADR0/ together with BHEN/ determines the type of byte transfer</td></tr>
<tr><td>ADR1/ through ADRF/</td><td>Fifteen lines that specify one of 64K byte locations within a memory block</td></tr>
<tr><td>ADRE/ through ADR13/ (MSB)</td><td>Six lines that select a memory module block address</td></tr>
</table></td></tr>
<tr><td>RAM Inhibit (INH1/)</td><td>1</td><td>INH1/ is a negative-true signal used to inhibit memory read and write operations. The inhibited cycle is produced by asserting INH1/ at times determined by the operating mode:
a. In Read/Restore INH1/ must be asserted no later than 50 nanoseconds after the leading edge of MRDC/.
b. In Delayed Write, INH1/ must be asserted no later than 50 nanoseconds after the leading edge of MWTC/.
c. In Advance Write mode, INH1/ must be asserted no later than 600 nanoseconds after the leading edge of MWTC/.</td></tr>
<tr><td>ROM Inhibit (INH2/)</td><td>1</td><td>INH2/ is normally used in systems employing an auxilary ROM which overlays both ROM and RAM, or PROM (memory with write protect). INH2/ is functionally the same as INH1.</td></tr>
</table>

Table 2-1. Input/Output Signals (contd)

<table>
<tr><th>Signal</th><th>No. of Lines</th><th>Description</th></tr>
<tr><td>Byte High Enable (BHEN/)</td><td>1</td><td>BHEN/ together with ADR0/, specify the source and destination of transferred data byte(s), as listed below.
<table>
<tr><th>BHEN/</th><th>ADR0/</th><th>Transfer</th></tr>
<tr><td>H</td><td>H</td><td>Low (even) byte (bits 0 through 7) on the low byte data lines (DAT0/ through DAT7/).</td></tr>
<tr><td>H</td><td>L</td><td>High (odd) byte (bits 8 through F) on the low data lines (DAT0/ through DAT7/).</td></tr>
<tr><td>L</td><td>H</td><td>(16 bits transfer) bits 0–F to DAT0/ through DATF/</td></tr>
<tr><td>L</td><td>L</td><td>High (odd) byte (bits 8 through F) on high byte data lines (DAT8/ through DATF/).</td></tr>
</table>
BHEN/ must be asserted 50 nanoseconds before MRDC/ or MWTC/ and must remain stable until 50 nanoseconds after MWTC/ or MRDC/ is removed.</td></tr>
<tr><td>Data Bus (DAT0/ – DATF/)</td><td>16</td><td>Sixteen bidirectional data lines which carry both read and write data between the memory module and the external system. For delayed write operations, data must be valid on the data bus 50 nanoseconds before MWTC/. In advance write mode, data must be valid on the data bus no later than 500 nanoseconds after the leading edge of MWTC/. Write data must remain stable for a minimum of 300 nanoseconds (250 nanoseconds after MWTC/). For read-restore operations, stable read data is available on the data bus 425 nanoseconds after MRDC/ is asserted. Read data on the data bus is not valid until 65 nanoseconds after MRDC/ is removed.</td></tr>
<tr><td>Transfer Acknowledge (XACK/)</td><td>1</td><td>XACK/ is a negative-true output signal which indicates to the external system that read data is available on the data bus (read-restore) or write data has been accepted from the data bus (clear-write). XACK/ is output no later than 400 nanoseconds after the leading edge of MWTC/ or MRDC/. In advance mode, XACK/ occurs no later than 940 nanoseconds after the leading edge of MWTC/, provided that the previous memory cycle has already finished. The XACK/ signal remains active until the command is removed. Once the command is negated, XACK/ is removed within 65 nanoseconds.</td></tr>
<tr><td>Advance Acknowledge (AACK/)</td><td>1</td><td>Advance acknowledge (AACK/) is a negative-true output signal which is user adjustable if the signal is set at its nominal time. It will occur no later than 120 nanoseconds after the leading edge of MRDC/ (read/restore mode). In delayed write mode, AACK/ occurs no later than 120 nanoseconds after the leading edge of MWTC/. In advance write operations, AACK/ occurs no later than 650 nanoseconds after the leading edge of MWTC/, provided that the previous memory cycle has already finished. The AACK/ signal remains active until the command is removed. Once the command is negated, AACK/ is removed within 65 nanoseconds.</td></tr>
</table>

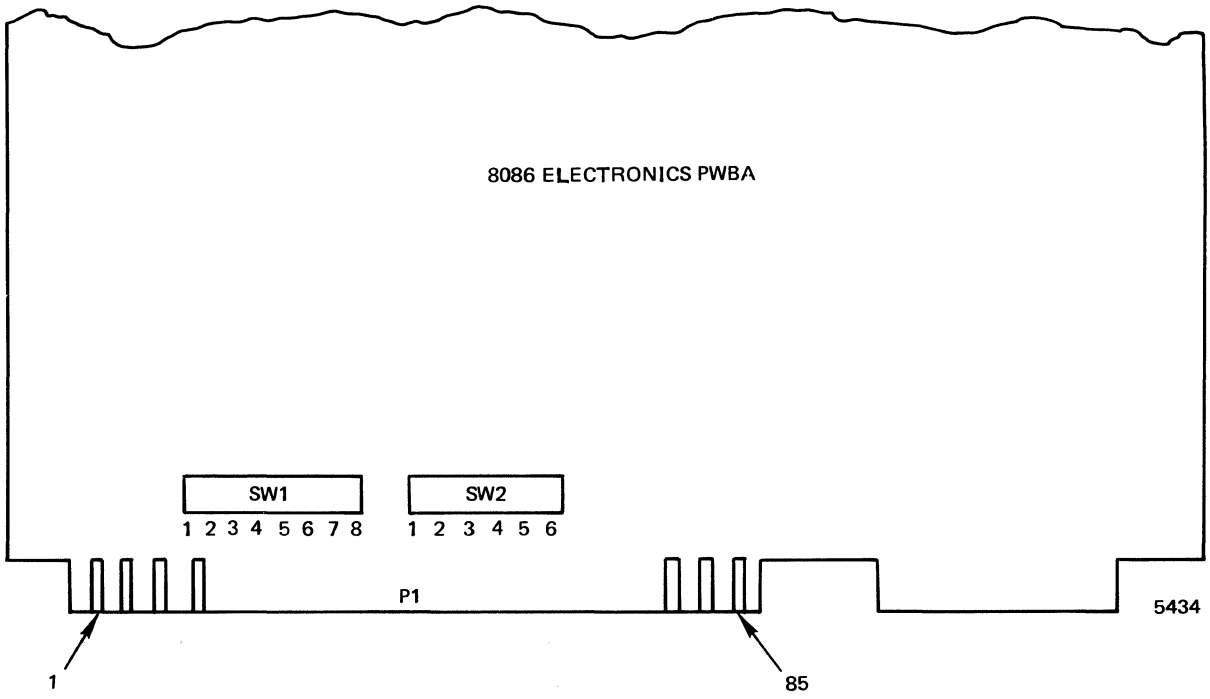


Figure 2-2. Switch Locations

Table 2-2. Memory Connector (P1) Pin Assignments

	Component Side		Circuit Side	
	Pin	Signal	Pin	Signal
Address	43	ADRE/	44	ADRF/
	45	ADRC/	46	ADRD/
	47	ADRA/	48	ADRB/
	49	ADR8/	50	ADR9/
	51	ADR6/	52	ADR7/
	53	ADR4/	54	ADR5/
	55	ADR2/	56	ADR3/
	57	ADR0/	58	ADR1/
Data	59	DATE/	60	DATF/
	61	DATC/	62	DATD/
	63	DATA/	64	DATB/
	65	DAT8/	66	DAT9/
	67	DAT6/	68	DAT7/
	69	DAT4/	70	DAT5/
	71	DAT2/	72	DAT3/
	73	DAT0/	74	DAT1/
Power Supplies	75	GND	76	GND
	77	---	78	---
	79	---	80	---
	81	+5V	82	+5V
	83	+5V	84	+5V
	85	GND	86	GND

	Component Side		Circuit Side	
	Pin	Signal	Pin	Signal
Power Supplies	1	GND	2	GND
	3	+5VI	4	+5VI
	5	+5V	6	+5V
	7	+12VI	8	+12V
	9	---	10	---
	11	GND	12	GND
Bus Controls	13	---	14	INIT/
	15	---	16	---
	17	---	18	---
	19	MRDC/	20	MWTC/
	21	---	22	---
	23	XACK/	24	INH1/
		---	26	INH2/
Spares	25	AACK/	28	ADR10/
	27	BHEN	30	ADR11/
	29	---	32	ADR12/
	31	---	34	ADR13/
	33	---		
Interrupts	35	---	36	---
	37	---	38	---
	39	---	40	---
	41	---	42	---

Table 2-3. Module Select Switch Selection (64K Byte Boundaries)

Switch Position SW2						Starting Address		Ending Address	
ADR13	ADR12	ADR11	ADR10	ADRF	ADRE				
1	2	3	4	5	6	Hex	Decimal	Hex	Decimal
ON	ON	ON	ON	OFF	OFF	00000	0K	OFFFF	64K
ON	ON	ON	OFF	OFF	OFF	10000	64K	1FFFF	128K
ON	ON	OFF	ON	OFF	OFF	20000	128K	2FFFF	192K
ON	ON	OFF	OFF	OFF	OFF	30000	192K	3FFFF	256K
ON	OFF	ON	ON	OFF	OFF	40000	256K	4FFFF	320K
ON	OFF	ON	OFF	OFF	OFF	50000	320K	5FFFF	384K
ON	OFF	OFF	ON	OFF	OFF	60000	384K	6FFFF	448K
ON	OFF	OFF	OFF	OFF	OFF	70000	448K	7FFFF	512K
OFF	ON	ON	ON	OFF	OFF	80000	512K	8FFFF	570K
OFF	ON	ON	OFF	OFF	OFF	90000	576K	9FFFF	640K
OFF	ON	OFF	ON	OFF	OFF	A0000	640K	AFFFF	704K
OFF	ON	OFF	OFF	OFF	OFF	B0000	704K	BFFFF	768K
OFF	OFF	ON	ON	OFF	OFF	C0000	768K	CFFFF	832K
OFF	OFF	ON	OFF	OFF	OFF	D0000	832K	DFFFF	986K
OFF	OFF	OFF	ON	OFF	OFF	E0000	896K	EFFFF	960K
OFF	OFF	OFF	OFF	OFF	OFF	F0000	960K	FFFFF	1024K

Table 2-4. Module Select Switch Selection (16K Byte Boundaries)

Switch Position SW2						Starting Address		Ending Address	
ADR13	ADR12	ADR11	ADR10	ADRF	ADRE				
1	2	3	4	5	6	Hex	Decimal	Hex	Decimal
ON	ON	ON	ON	ON	ON	00000	0K	03FFF	16K
ON	ON	ON	ON	ON	OFF	00000	0K	07FFF	32K
ON	ON	ON	ON	OFF	ON	00000	0K	0BFFF	48K
ON	ON	ON	ON	OFF	OFF	00000	0K	0FFFF	64K
ON	ON	ON	OFF	ON	ON	04000	16K	13FFF	80K
ON	ON	ON	OFF	ON	OFF	08000	32K	17FFF	96K
ON	ON	ON	OFF	OFF	ON	0C000	48K	1BFFF	112K
ON	ON	ON	OFF	OFF	OFF	10000	64K	1FFFF	128K
OFF	OFF	OFF	OFF	ON	ON	E4000	912K	F3FFF	976K
OFF	OFF	OFF	OFF	ON	OFF	E8000	928K	F7FFF	992K
OFF	OFF	OFF	OFF	OFF	ON	EC000	944K	FBFFF	1008K
OFF	OFF	OFF	OFF	OFF	OFF	F0000	960K	FFFFF	1024K

Table 2-5. Write Protect/Access Inhibit Address Selection

SW1-5	SW1-6	Access Inhibit	Write Protect
OFF/	OFF	NO	NO
OFF/	ON	NO	NO
ON	OFF	YES	NO
ON	ON	NO	YES

NOTE: It is possible to disable Access Inhibit or Write Protect by placing SW1-5 to OFF position, without having A0 change any other switch settings.

2.4 OPERATION

Because of the all-electronic nature of the memory module, manual operation consists primarily of energizing the unit in readiness for functional operation. There are no operator controls or indicators on the module.

2.5 OPERATOR MAINTENANCE

The memory module does not require routine operator maintenance. However, certain preventive maintenance operations, to be performed by a service technician, are recommended for continued trouble-free operation of the equipment. These are described in Section IV, Maintenance Procedures.

SECTION III
PRINCIPLES OF OPERATION

3.1 GENERAL

This section describes the principles of operation and major circuit functions of the MCM-8086 Microcomputer Core Memory module.

3.2 FUNCTIONAL DESCRIPTION

Figure 3-1 is a functional block diagram of the memory module. The module consists of several circuit groups which perform various functions. The following paragraphs describe these functions.

3.2.1 Timing and Control

Memory module timing is established by a Johnson Counter enabled by the memory cycle commands. The timing and control signals are sent to the X/Y current source, data register, sense amplifiers, and X/Y drive and sink decoders to activate them in the proper logic sequences.

3.2.2 Address Register and Decode

Fifteen address bits (1 through 9 and A through F) are used to select specified data word locations of the core array. The address is separated into four groups and applied to the appropriate decoders for activation of selected X and Y drive and sink switches.

3.2.3 X/Y Drive and Sink Switches

The X and Y drive and sink switches route the necessary current for selecting core locations during read and write operations. During the read segment of the memory cycle, read timing is supplied to all drive and sink switches. Read current is enabled in the switch combinations that correspond to the addressed core locations, allowing current to flow through the sink switch, core stack, and drive switch to the read current source.

During the write segment of a memory cycle, the applicable switches remain activated, and write current is enabled, permitting current to flow through the core stack in a direction opposite to that of the read current. By employing the previously described drive/sink switch configuration in both the X and Y directions, applying half currents in each direction, specific cores may be selected and magnetically modified in either read or write operations.

3.2.4 X/Y Current Source

The X/Y current source supplies a constant current necessary for the magnetic modification of the cores. The X/Y current source is enabled by the timing and control circuits.

3.2.5 Sense/Inhibit Circuits

The inhibit circiuts are used in write operations if a ZERO is to be written into an addressed core. Figure 3-2 illustrates X, Y, and sense/inhibit currents during read and write operations. During a write operation, half-write currents flow in the X and Y lines of the addressed core. If a ZERO is to be written, the inhibit driver, enabled by the data bit, allows half-currents to flow in the sense/inhibit lines, through the core, in a direction opposite to that of the parallel Y line. The inhibit and Y half currents cancel each other; thus, the core remains in the ZERO state (Figure 3-2a). If a ONE is to be written, no inhibit current flows, allowing the X and Y half write current to combine and change the core to the ONE state (Figure 3-2b). The nonaddressed cores, receiving only half current, are unaffected, (i.e., do not undergo a change in magnetic state).

The sense circuits are used to detect data in the cores during read operations. During a read operation, half-read currents flow through the X and Y lines in a direction that will change the core to the ZERO magnetic state. If the core was originally storing a ZERO, no change in magnetic state will occur; thus, the sense circuit detects a ZERO (Figure 3-2c). If the core was originally storing a ONE, it will be switched to a ZERO. This reversal in magnetic state is impressed upon the sense/inhibit line and detected as a ONE by the sense amplifier (Figure 3-2d). Read timing allows the read data to reach the data register.

3.2.6 Data Register

The memory data register consists of sixteen flip-flops, each of which stores one bit of the data word. Read data from the sense amplifier is sent to that data register

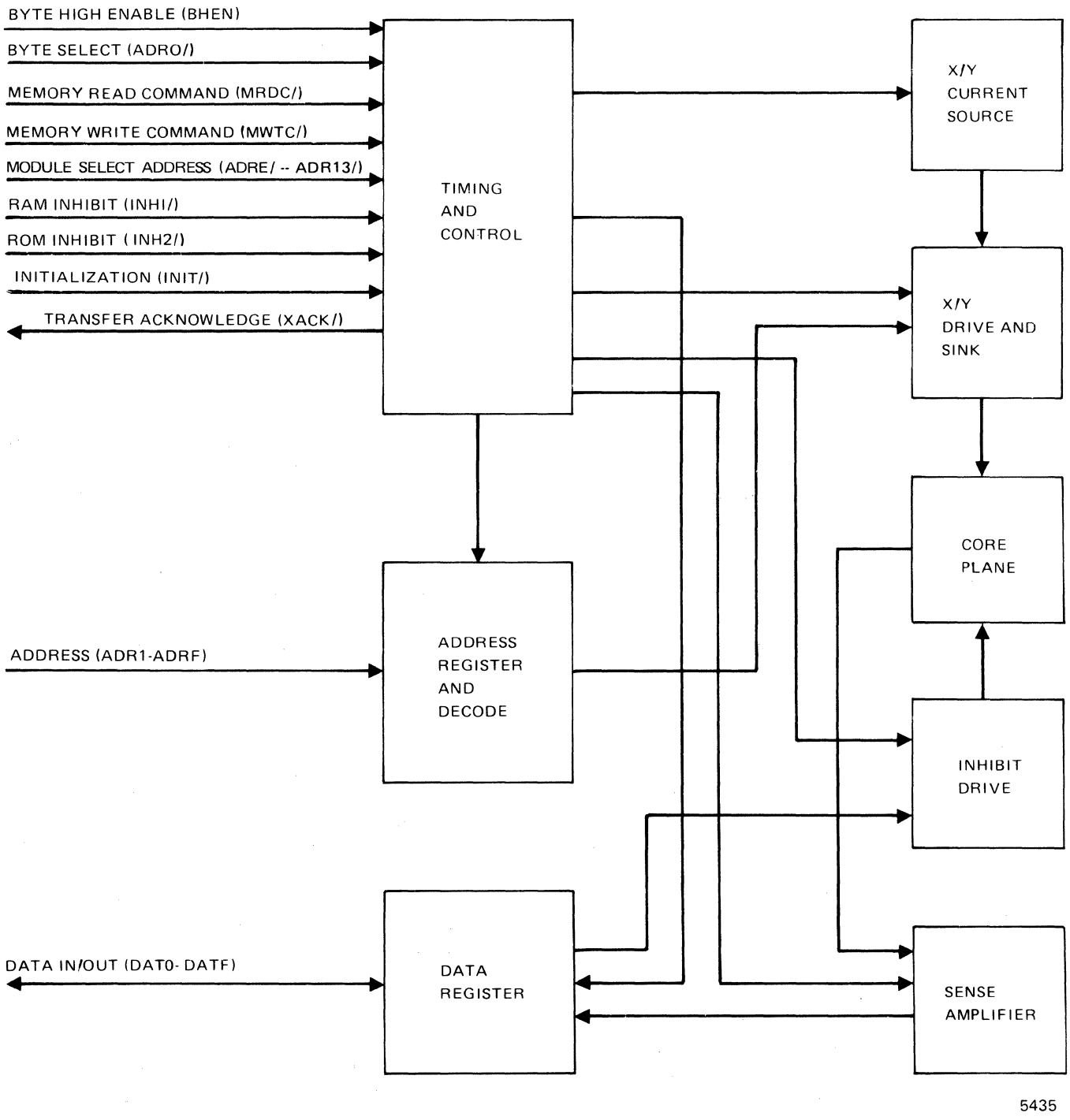


Figure 3-1. Functional Block Diagram

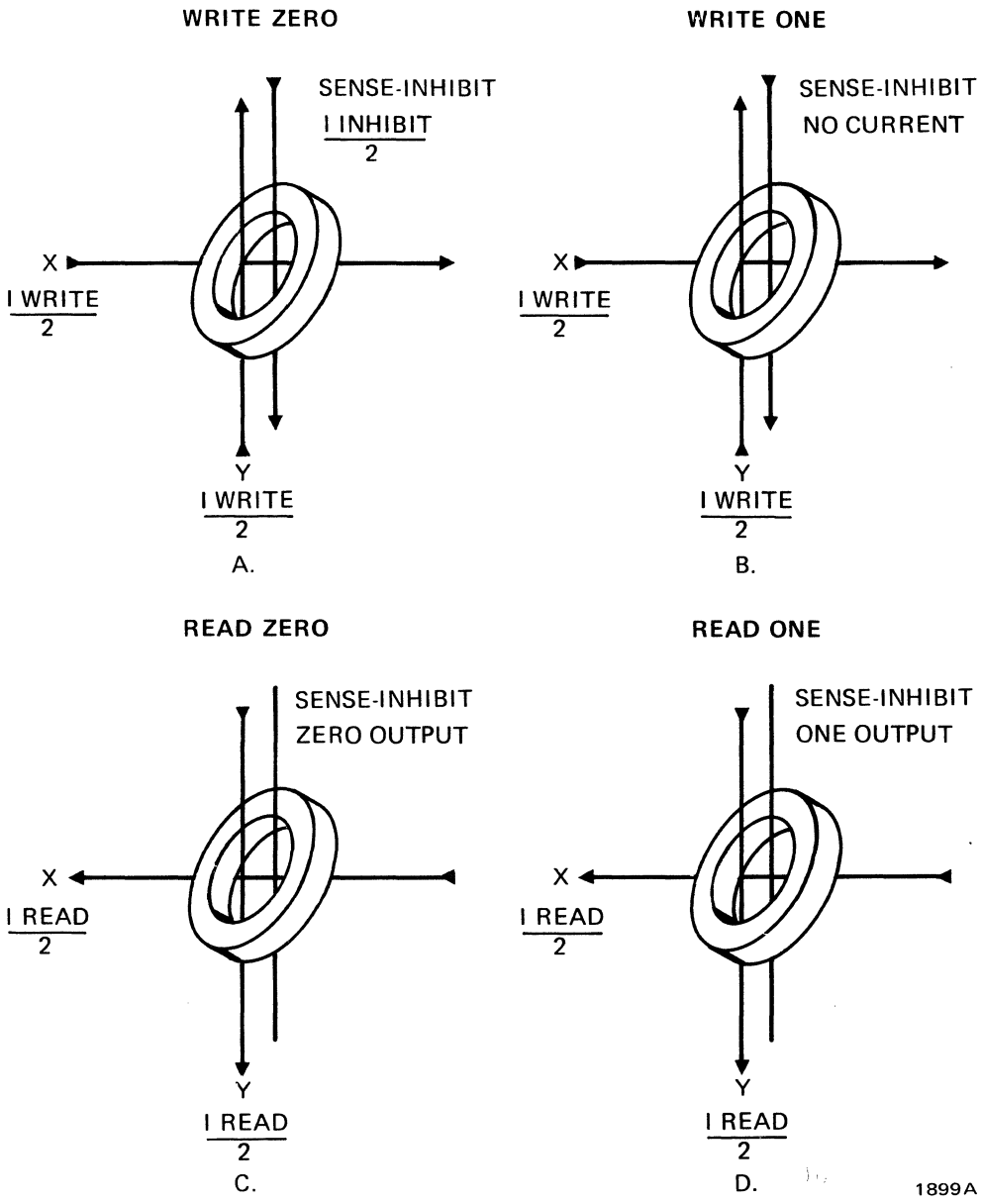


Figure 3-2. 3-Wire, 3-Dimensional Core Dynamics

so that it may be held until the data register receives the data out strobe. The data out strobe allows the temporarily stored data to reach the processor at the correct time.

3.3 OPERATIONAL DESCRIPTION

The following paragraphs describe the various operating modes of the MCM-8086 memory module. Timing diagrams accompanying the text provide support material.

3.3.1 Read-Restore Cycle

The function of a read-restore cycle is to output the contents of the magnetic cores at the address specified by the external system, and then to restore the data to the original state in the core stack.

A negative transition to the low logic level on the MRDC/ line initiates a read-restore cycle. Figure 3-3 illustrates read-restore timing. The MRDC/ signal is applied to the memory, indicating to it that a memory location address has been placed on the system address lines. MRDC/ also specifies that the contents of the addressed location are to be read and placed on the data bus within 400 nanoseconds.

3.3.2 Clear-Write Cycle

During a clear-write cycle, the addressed word location is selected and cleared, and new data is stored at that address.

A negative transition to the low logic level on the MWTC/ line initiates the clear-write cycle, as shown in Figure 3-4. Assertion of MWTC/ indicates to the memory that the address of a memory location and the Write data has been placed on the system bus. MWTC/ specifies that the data word is to be written into the addressed memory location. Address and Write data are taken off the bus after negation of MWTC/.

3.3.3 Inhibit

The inhibit signal, when asserted, inhibits RAM/ROM read/write operations. The Inhibit cycle, shown in Figure 3-5, is asserted no later than 50 nanoseconds after the leading edge of MRDC/ (or MWTC/ delayed write mode), or no later than 600 nanoseconds after the leading edge of MWTC/ in advanced write mode. For active cycles (noninhibited) the inhibit is removed 50 nanoseconds before MRDC/ (or MWTC/ in delayed write mode) or no later than 500 nanoseconds after the leading edge of MWTC/ in advanced write mode.

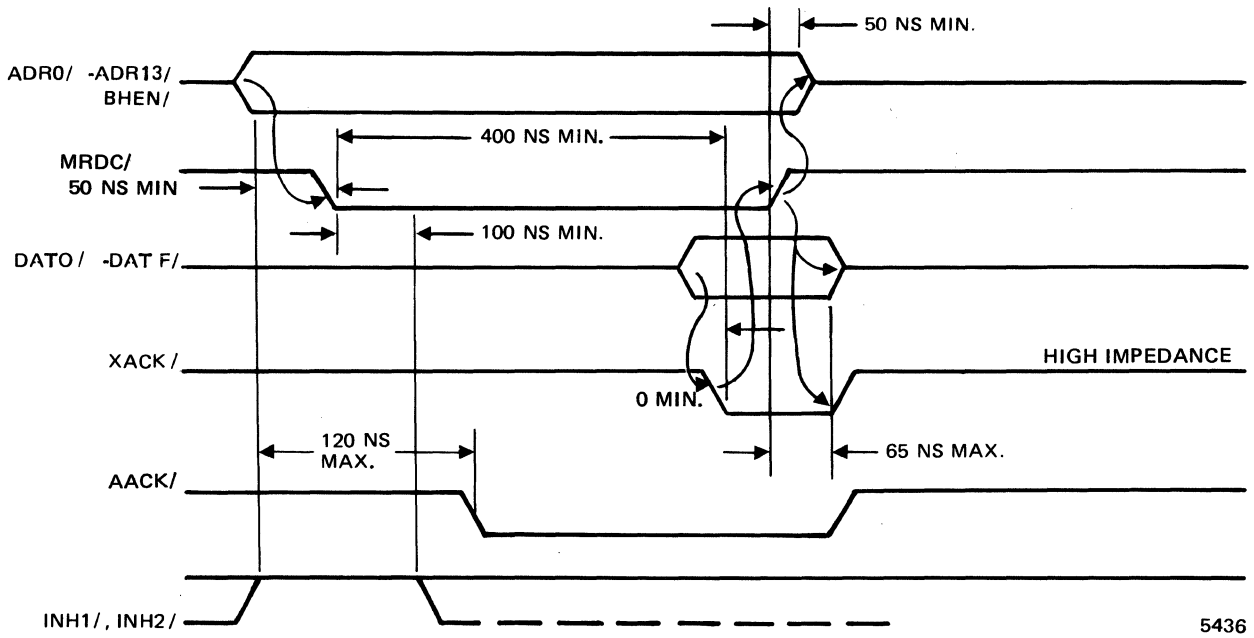


Figure 3-3. Read-Restore Timing

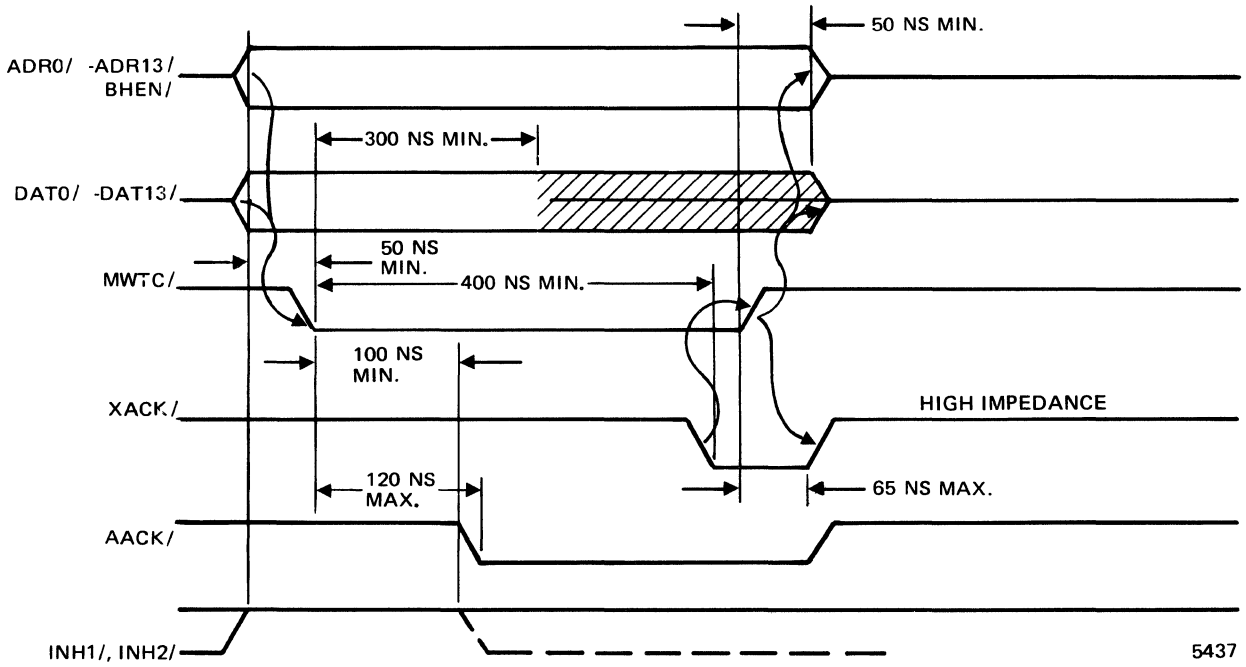


Figure 3-4. Clear Write Timing

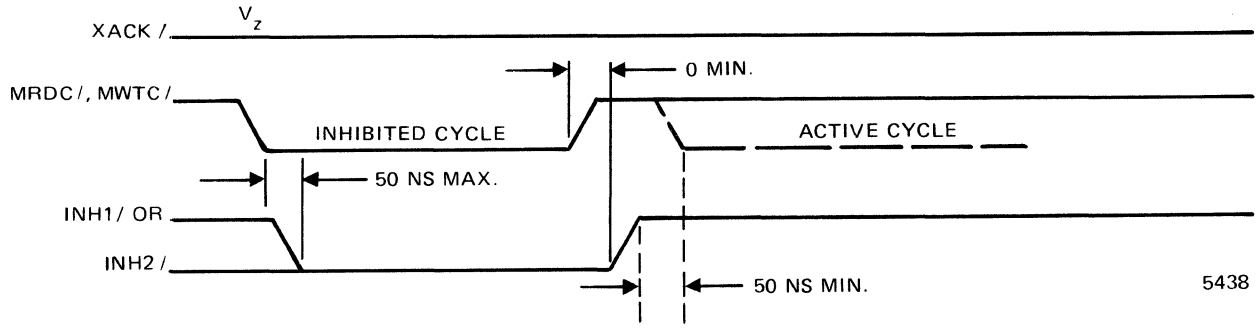
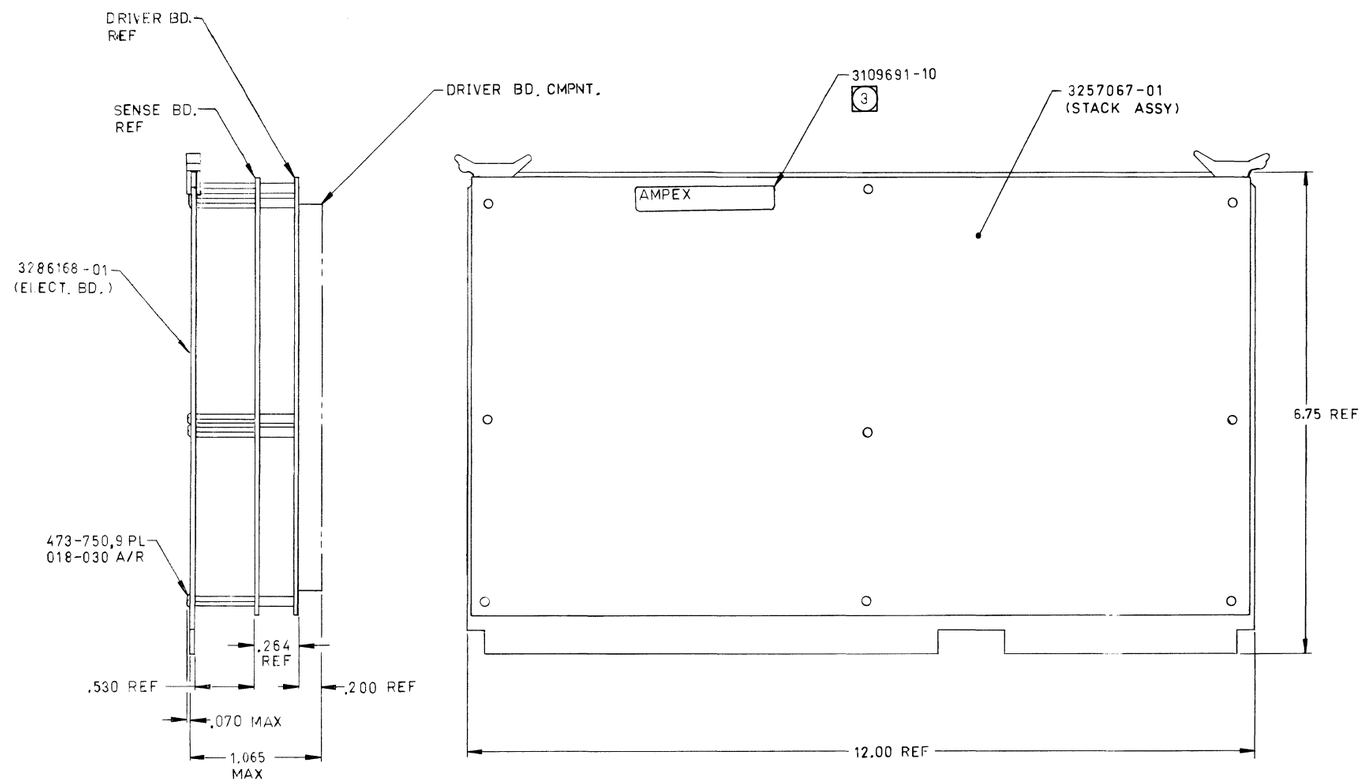


Figure 3-5. Inhibit Timing (Delayed Write Mode)

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 7102 (PROTO)			
B		PCR 38960			
C		PCR 39007			
D		PCR 39049			



| PIN ASSIGNMENT | | | | |

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 7167 (PROTOTYPE)	10-31-71		
B		PCR 39018	12-15-71		
C		PCR 39041	1-25-72		
(18)	D	PCR 39054	2-15-72		

(18) FOR REWORK INSTRUCTION TO PWBA USING ISS 'A' A/W SEE PCR39054.
(17) JUMPER TO BE DETERMINED IN TEST.
(16) INITIAL VALUE SHOWN FINAL VALUE TO BE DETERMINED IN TEST.
(15) ADD SLEEVING (600-237) TO ALL VERTICAL COMPONENTS.
(14) FOR MAX COMPONENT HEIGHT SEE TABLE 1.
(13) DIODES ARE MOUNTED WITH CATHODE END UP.
(12) VALUE TO BE SELECTED IN TEST.
11. POWER CONNECTION OF I.C.:—
FOR 16 PIN, 16 IS +5V, 8 IS GND.
FOR 14 PIN, 14 IS +5V, 7 IS GND.
10. ALL CAPACITORS ARE IN MICROFARADS, 50 V, +80%, −20%.
9. ALL RESISTORS ARE IN OHMS, 1/4W, 2%.
8. FOR SCHEMATIC SEE SH 4 THRU SH 14.
7. MAX SOLDER HEIGHT TO BE .070.
6. PLUS SIGN ON CAP INDICATES POSITIVE.
5. HEAVY LINE ON DIODE INDICATES CATHODE.
4. COMPONENT DES ARE FOR REF ONLY.
(3) MARK PART NO. AND ISSUE LTR PER AMPEX SPEC 3124500, PARA 3.1.
2. PART NO. TO BE 3286168-01.
1. ASSEMBLE PER AMPEX STANDARDS.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST ☒

3286074	MCM 8086
NEXT ASSY	USED ON
APPLICATION	

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INTERPRET DRAWING PER ANSI Y14.5
MATERIAL:
FINISH:

SIGNATURE		DATE
DRAWN BY	C. H. Ho	10-31-71
CHK BY	C.C. Fu	11-1-71
DFTG APVD		
ENGRG APVD		
AUTH BY		

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

PWBA
ELECTRONICS BD.
32K X 16

SIZE	CODE IDENT NO.	
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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—

PART NO.	REFERENCE DESIGNATION	DESCRIPTION
059-374	R111	54, 1%, 1W
076-619	R61, 88, 93, 141	1K
076-615	R104, 116, 121	470
076-605	R 20 THRU 27, 31 THRU 38, 66, 69, 113, 118	68
076-628	R 30, 46, 49, 88, 89	5.6K
076-608	R 39 THRU 42, 101	120
076-596	R 48, 68, 70	10
076-610	R11 , 123, 124	180
076-611	R 50, 95, 115 120), 135, 143	220
076-627	R53, 54, 84, 90, 73	4.7K
076-634	R 55, 56, 114, 119	22
076-621	R 132	1.5K
076-630	R59, 140, 75	8.2K
076-659	R 60	22K
076-606	R 62, 63, 100, 44	82
076-603	R 64, 65, 79, 82	47
076-620	R 52	1.2K
076-604	R 43	56
076-663	R 74, 76	100K
076-622	R 57, 77	1.8K
059-740	R80, 83	.237, 1%, 1W
076-613	R10, 51, 107, 109, 122	330
076-624	R 86	2.7K
076-660	R 87	33K
076-631	R 91	10K
076-629	R92	6.8K
076-623	R 94	2.2K
076-625	R 110, 129, 72	3.3K
059-537	R 112, 117, 126, 105	7.15, 1%, 1W
076-609	R 29	150, 2%
059-783	R1 THRU 8, 12 THRU 19	39, 1%, 1W
076-616	R45, 99, 125, 131	560
064-447	C93	1500pF, 10%
——	R 9, 28, 47, 108, 134, 137, 139	L. S. R.
076-607	R 96, 97, 98, 106, 127, 128, 136, 138, 142	100
064-443	C 1 THRU 32, 49 THRU 59, 61 THRU 81, 83 THRU 92, 94, 98, 100, 102 THUR 107 109 THRU 112, 138	.47
064-450	C 33 THRU 48	4700pF, 50V, 10%
064-467	C152	330pF, 100V, 5%
064-448	C 101	2200pF, 50V, 10%
064-446	C 95, 96	1000pF, 50V, 10%
064-465	C 115, 151	150pF
037-892	C 137	47, 20V, 20%
037-931	C 121 THRU 132, 135, 150, 139, 140, 149, 134	6.8, 35V, 20%
037-954	C 141 THRU 148, 120, 133	22, 15V, 20%
064-458	C97	.1μF, 20%
3286093-01	L1	51 μH
——	C60, 82	L.S.C.
3286094-01	L2, 3, 4	94μH
037-936	C136	22, 35V, 20%
064-464	C116	100pF
064-468	C114	470pF, 100V, 5%

PART NO.	REFERENCE DESIGNATION	DESCRIPTION
580-617	U 1, 2, 3, 4, 7, 8, 9, 10	Q2T3725
3275600-01	U 11 THRU 18	XFMR 1:1
587-500	U 19 THRU 22, 25 THRU 28, 41	74S38N
587-751	U 23,	74S08N
589-404	U 24	74LS352N
586-830	U 5, 30, 32, 36, 34	74S00N
587-533	U 29, 31, 33, 35, 57, 65	74LS04N
3275801-02	U 37,	XFMR 1:1
587-499	U 38, 6	74S32N
587-277	U 39	74S02N
587-017	U 40	74S03N
587-510	U 42, 69	74LS00N
586-831	U 44	74S04N
587-282	U 45	74S260N
587-755	U 46	74LS85N
587-895	U 47, 52, 55, 56	74LS164N
587-569	U 48	8T98
587-479	U 49	74128N
587-814	U 50, 51	74LS283N
589-752	U 54, 58	74LS373N
587-366	U 59 THRU 64	8T26A
589-369	U 67	74LS156N
589-444	U 68	SG3524J
587-934	U 71	LM339
586-890	U 73	7417N
3275801-01	U 74, 70	XFMR 1:1
3275803-01	U 72	XFMR 10:7
580-789	Q 1, 2, 19	2N3467
580-790	Q 3, 4	2N4014
* 580-891	Q6, 8	2N4232A
580-872	Q14, 15, 20, 21, 22, 23	2N3725A
580-624	Q 10, 13, 16, 18	2N2907A
014-581	Q7, 11, 12, 17	2N2369A
068-078	L5, 6	68μH
013-224	VR1, 3	1N754A
013-358	VR 2, 4	1N751A
581-403	CR1 THRU 52, 54, 55, 56, 57, 58, 61 THRU 63, 65 THRU 80	CD6030-2
581-334	CR 59, 60	UTR3305
587-566	U43	74S37
581-557	SR 1 THRU 18	SCHOTTKY
039-126	RM 1, 2	CD6613-04
039-125	RM3	CD6613-03
3286068-01	T 1	X'FMR
076-778	R58	7.5K
119-759	SW 2	SWITCH
119-575	SW 1	SWITCH
570-258	DL 1	DELAY LINE
587-534	U53	74LS08
589-116	U 75	26S02

LAST USED	NOT USED
CR80	CR53, 64
C152	C117 THRU C119, C113
DL 1	—
L6	—
Q23	Q5, 9
R143	R67, 71, 78, 81, 130, 133
RM3	—
SR18	—
SW2	—
T17	—
U75	U66
VR4	—

NOT REQ'D
C93, C108, R102, R103

* ALTERNATE PART USE 579-088 (2N4233A)

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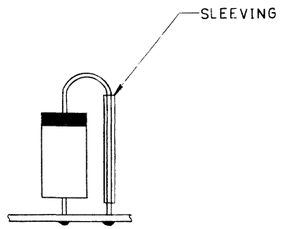
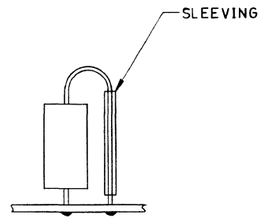


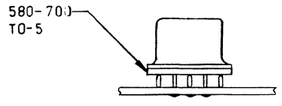
TYP DIODE MTG (15) (13)

(FOR CR49 THRU CR56, CR59 THRU CR63 CR65 THRU CR67, CR76 THRU CR79, SR17, SR18, VR2, VR3, VR4)



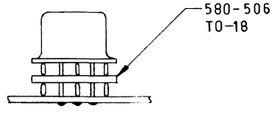
TYP RESISTOR MTG (15)

(FOR R39 THRU R66, R68 THRU R70, R72 THRU R77, R79, R80, R82 THRU R101, R104 THRU R109, R113 THRU R116, R118 THRU R124, R129 R130, R131, R134 THRU R137, R141 THRU R143.)



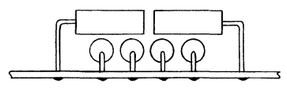
TYP TRANSISTOR MTG

(FOR Q1, Q2, Q14, Q15, Q19 THRU Q23)



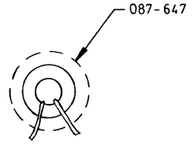
TYP TRANSISTOR MTG

(FOR Q3, Q4, Q7, Q10, Q11, Q12, Q13, Q16, Q17, Q18)



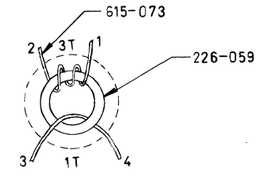
TYP CAPACITOR MTG

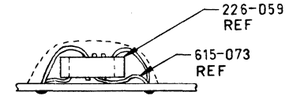
(FOR C1 THRU C32)



TYP INDUCTOR COATING

(FOR L1 THRU L4)





VIEW E (SEE SH 15)

(TYP FOR T2 THRU T17)

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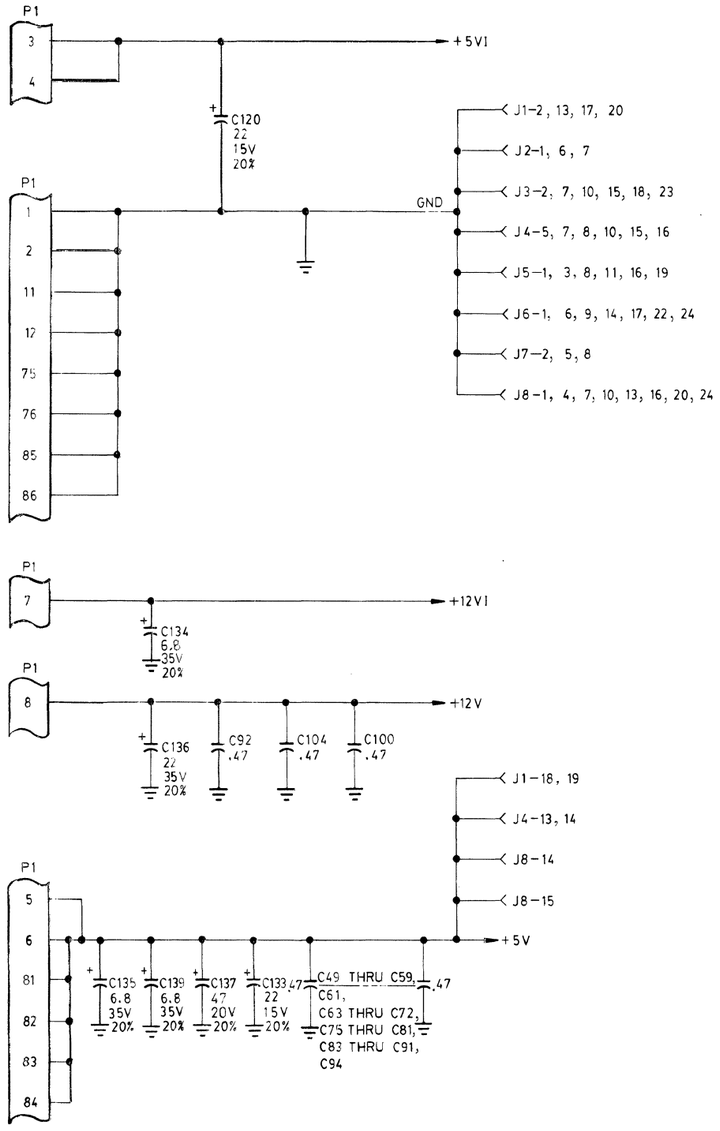

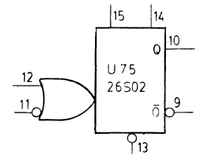

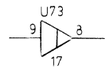

SPARE GATES

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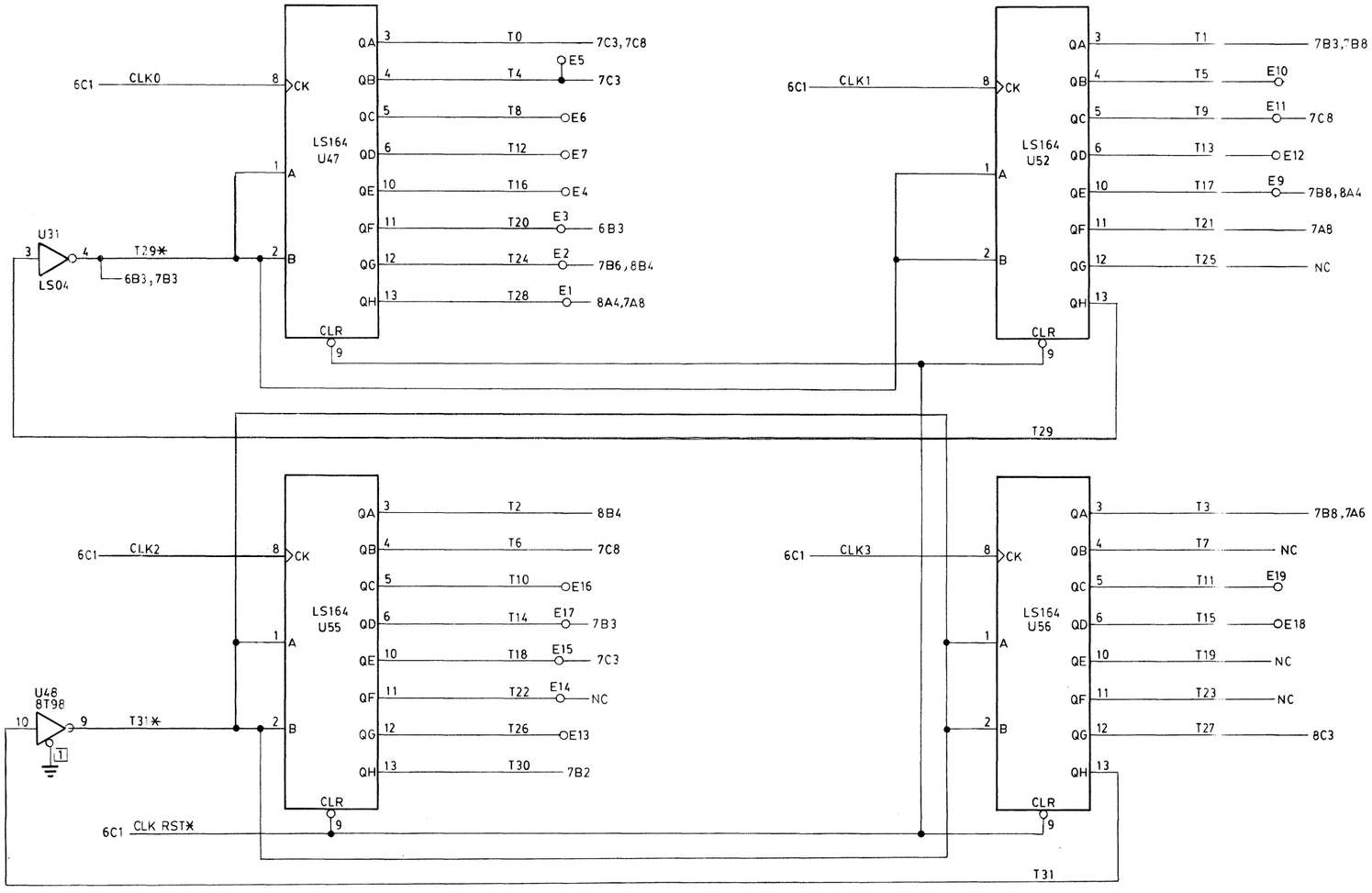

SHIFT REGISTER

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—

MODULE SELECT

WRITE PROTECT (ACCESS INHIBIT)

ADDRESS LATCH

CLK GEN

ADDRESS & CONTROL

SIZE	CODE IDENT NO.	
D	09150	3 2 8 6 1 6 8
SCALE NONE		SHEET 6 OF 15

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REVISIONS					
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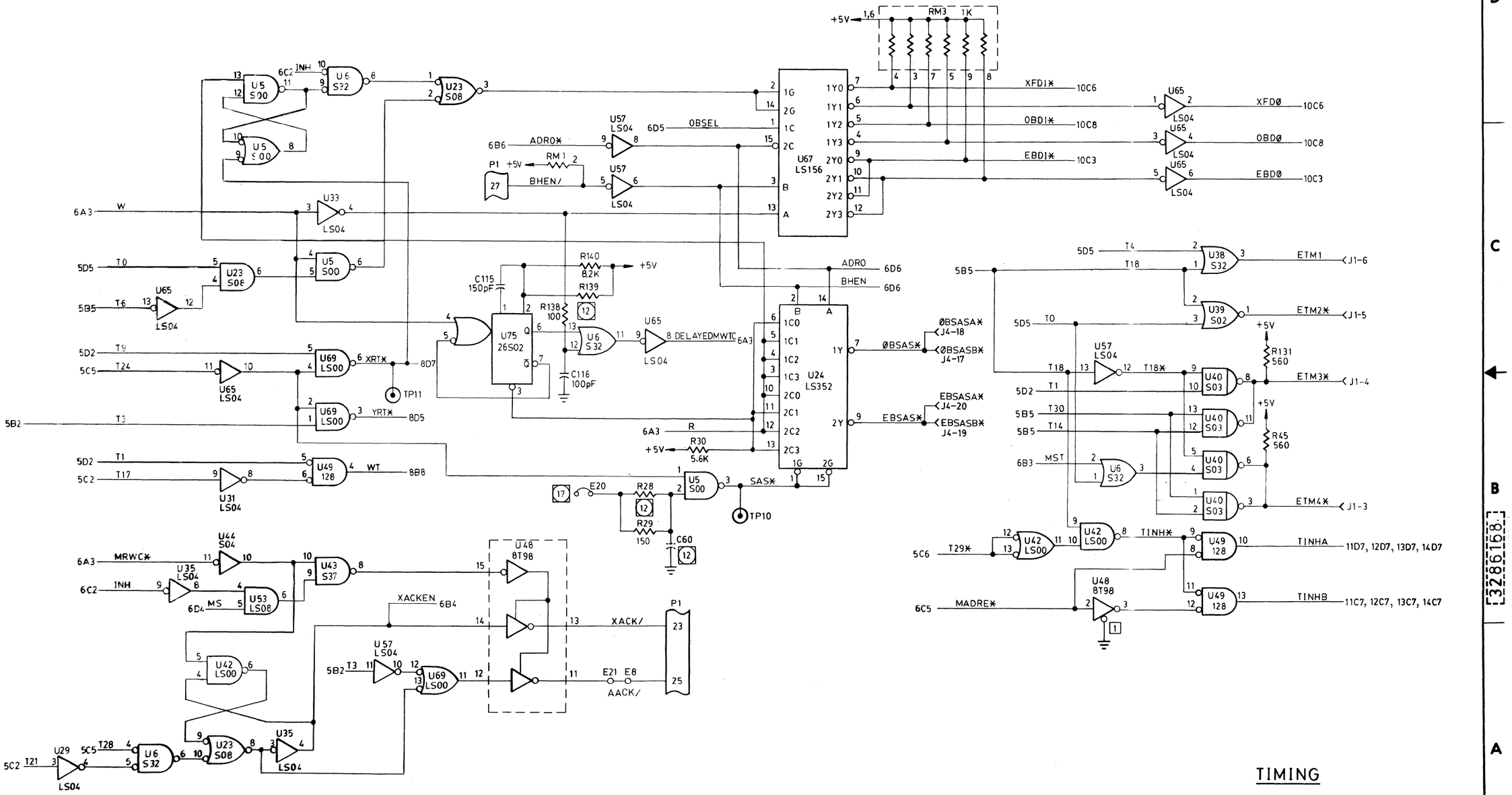

TIMING

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REVISIONS					
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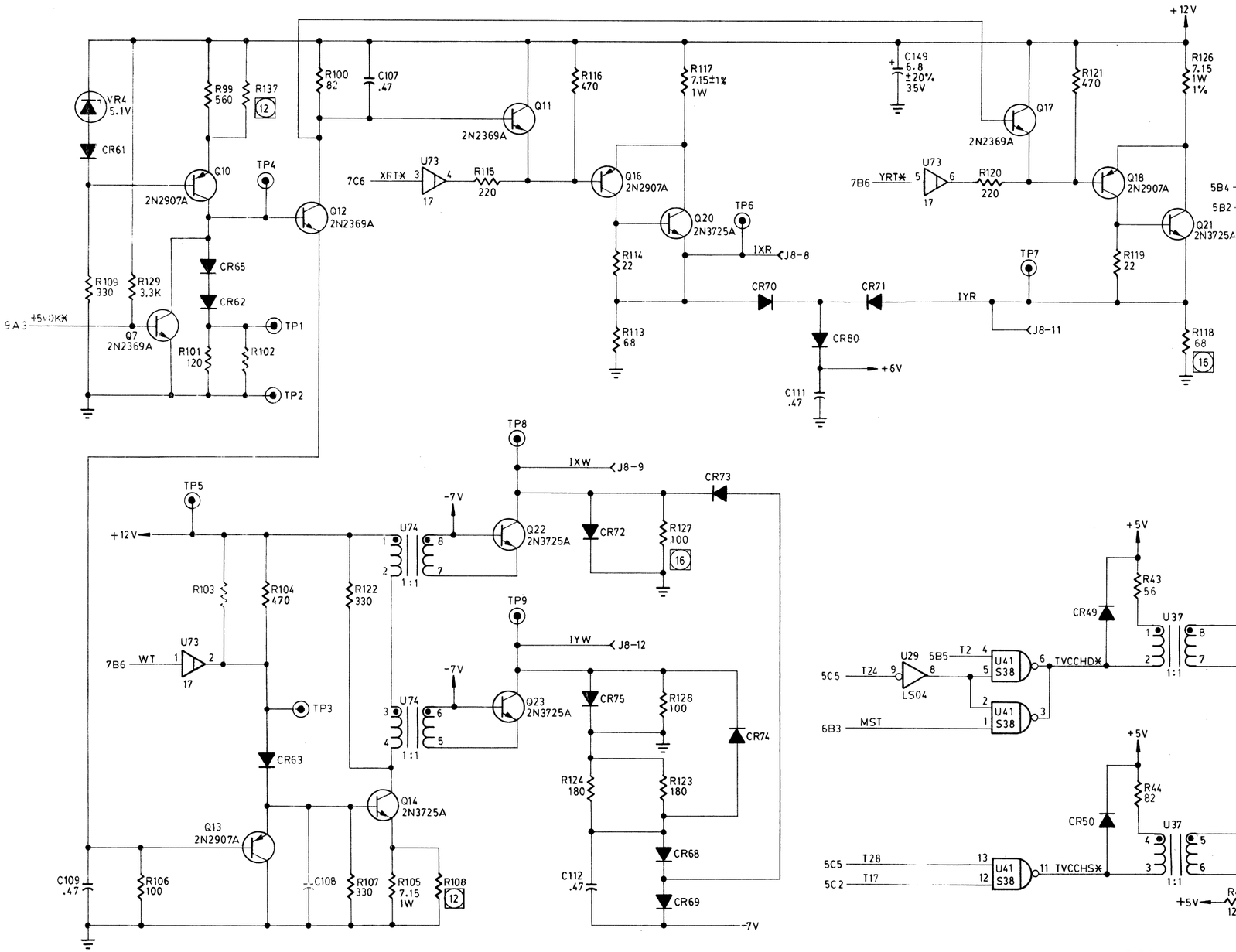

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SCALE NONE		SHEET 8 OF 15

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFTG	CHK	ENGRG
D		SEE SH 1			

VR2 5.1V
CR51
C102 .47
R56 22
R55 22
C140 6.8 35V 20%
R134
R58 7.5K
R60 22K
R57 1.8K
R53 4.7K
R54 4.7K
C95 .001
C96 .001
U68 SG3524
VCC
VREF
INV
N.I.
COMP
RT
CT
GND
CA
EA
CB
EB
CL+
CL-
SHUT DOWN
NC
CR52
C138 .47
C97 .1
R61 1K
R59 8.2K
C93 1500pF
R63 82
R82 47
R79 47
R62 82
R69 68
R68 10
R66 68
R70 10
R64 47
R65 47
R83 .237 1W 1%
R80 .237 1W 1%
R96 3.3K
C101 2200pF
SR18
SR17
U70 1:1
L5 68µH
L6 68µH
Q4 2N4014
Q3 2N4014
Q8 2N4232A
Q6 2N4232A
CR79
CR78
T1
+12V
CR76
CR77
UTR3305 CR59
UTR3305 CR60
CR56
CR55
CR57
CR58
L4 94µH
R135 220
L1 51µH
L2 94µH
L3 94µH
+13V
C150 6.8 35V
VXR J7-7
VYR J8-3
J8-5
J8-6
-7V
J4-11
J4-12
-5V
+6V
C143 22 15V
C144 22 15V
C145 22 15V
C146 22 15V
C148 22 15V
C105 .47
C106 .47
C62 .47
C141 22
C103 .47
C142 22 15V
C147 22 15V
R111 54 1W 1%

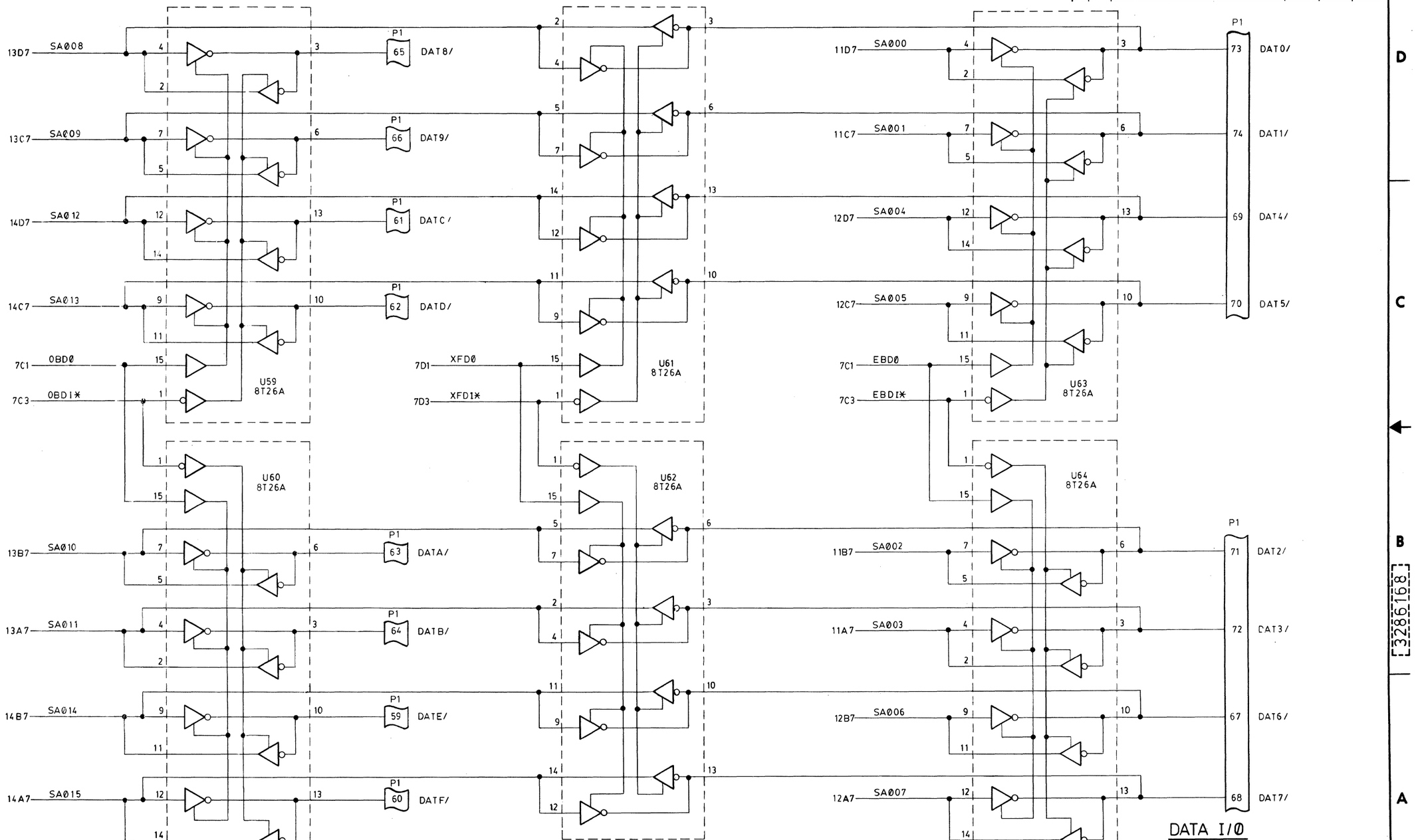
CONVERTER

+12V1
R11 1F0
R10 330
VTH J4-9
VR1 6.8V
R9
VTH

+12V
R95 220
R92 6.8K
CR54
+5V
VR3 6.8V IN754A
+6.8VR
C98 .47
R85 5.6K
R86 2.7K
R93 1K
R84 4.7K
R74 100K
R77 1.8K
PSØK 6B4
R94 2.2K
R91 10K
R75 8.2K
R72 3.3K
-7V
U71 LM339
R90 4.7K
R89 5.6K
R87 33K
R73 4.7K
R88 1K
R76 100K
R132 1.5K
U33 LS04
+5VOK* 8C8

PSØK

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—



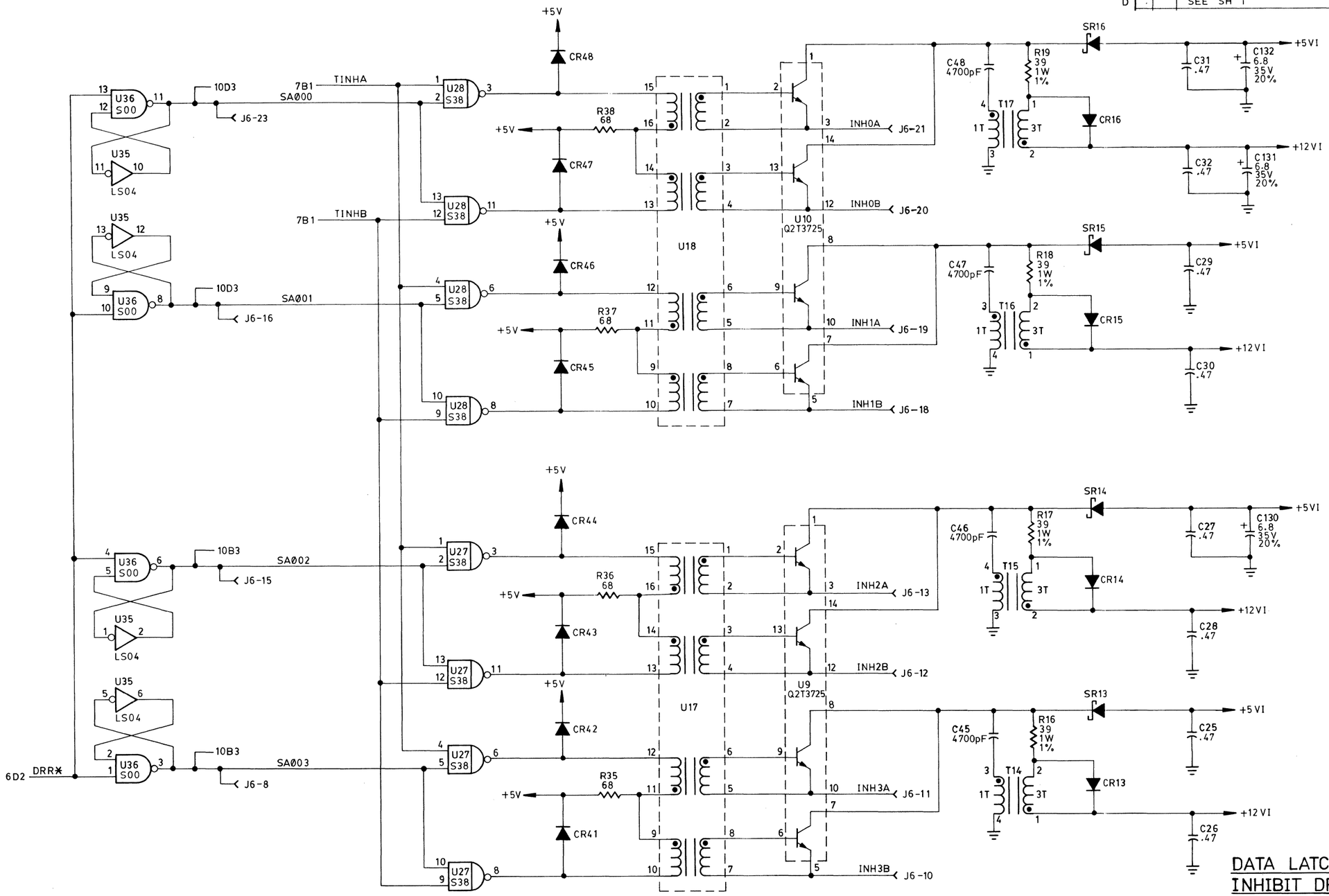
DATA I/Ø

SIZE	CODE IDENT NO.	
D	09150	3 2 8 6 1 6 8
SCALE NONE		SHEET 10 OF 15

UC-2804-08 (REV. NOV. 72)
PRINTED IN U.S.A.

3286168

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D	.	SEE SH 1	—	—	—



DATA LATCHES & INHIBIT DRIVERS

SIZE	CODE IDENT NO.	
D	09150	3 2 8 6 1 6 8
SCALE NONE		SHEET 11 OF 15

UC-3984-08 (REV. NOV. 72)
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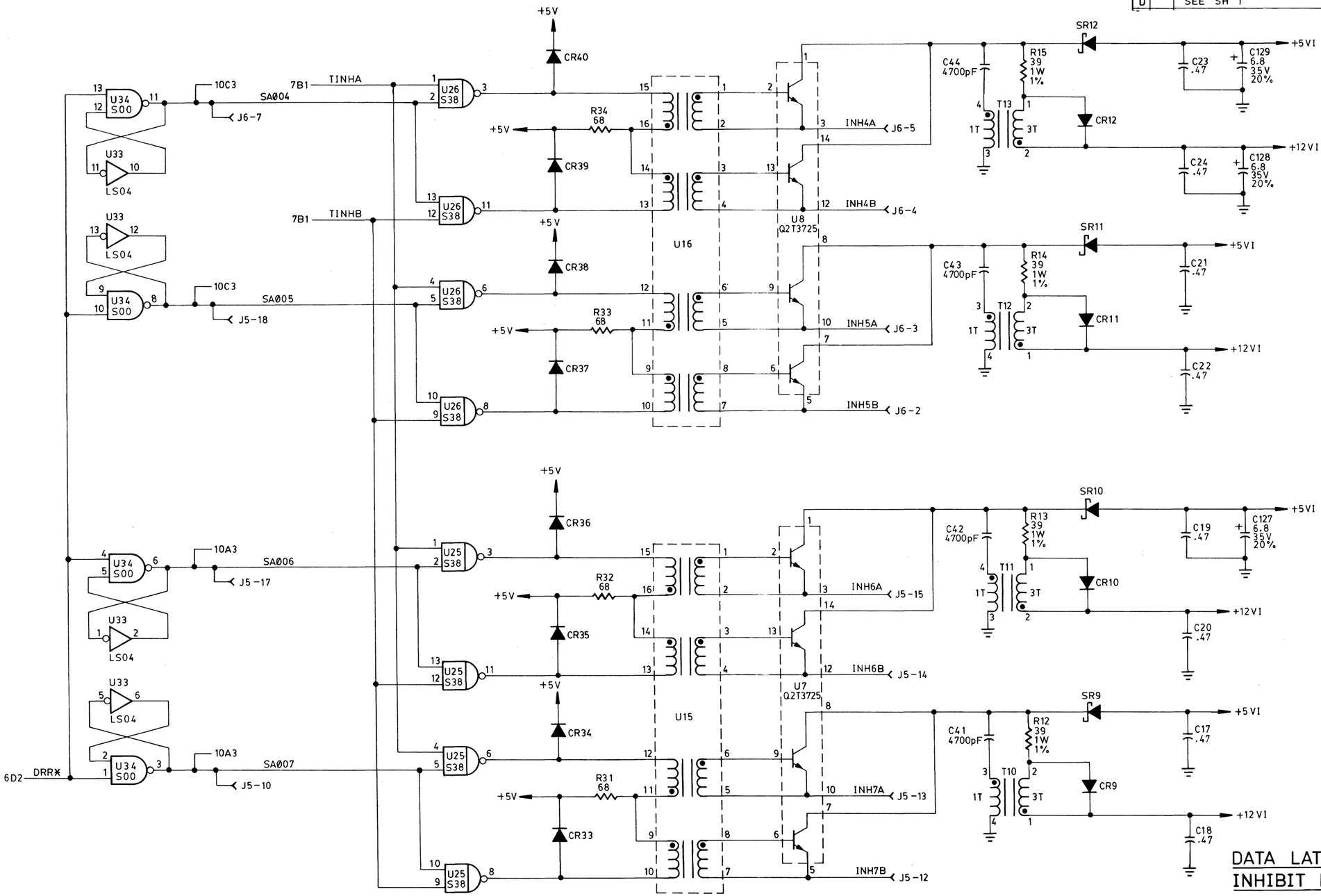
3286168

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—



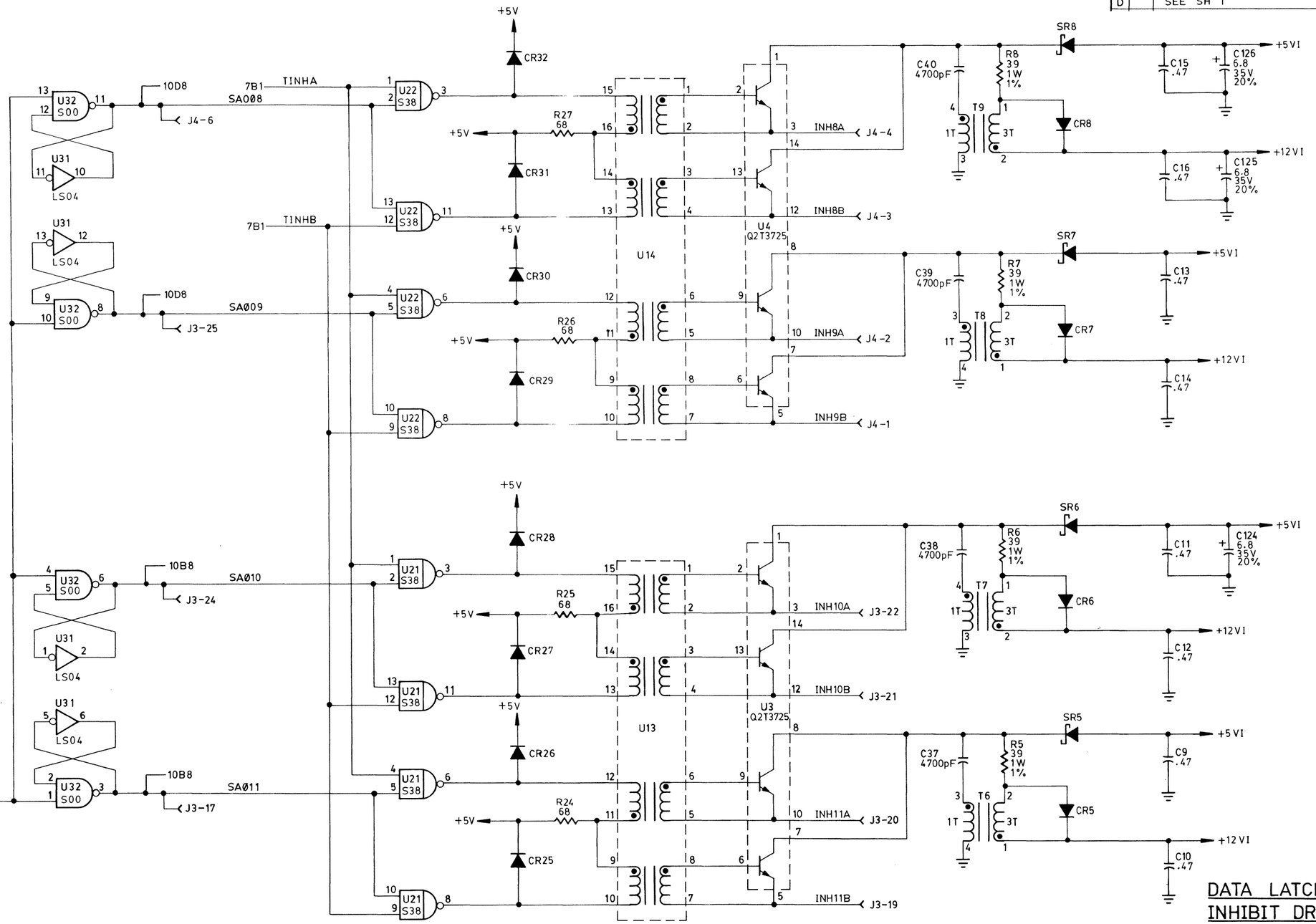
DATA LATCHES & INHIBIT DRIVERS

SIZE	CODE IDENT NO.	
D	09150	3 2 8 6 1 6 8

SCALE NONE — SHEET 12 OF 15

UC-3984-06 (REV. NOV. 70)
PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—



DATA LATCHES & INHIBIT DRIVERS

SIZE	CODE IDENT NO.	
D	09150	3 2 8 6 1 6 8

SCALE NONE SHEET 13 OF 15

UC-2804-08 (REV. NOV. 72) PRINTED IN U.S.A.

3286168

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—

U30 S00 U29 LS04 U20 S38 U19 S38 U12 U11 U2 Q2T3725 U1 Q2T3725

10C8 SA∅12 J3-16 7B1 TINHA 10C8 SA∅13 J3-9 10A8 SA∅14 J3-8 6D2 DRR✕ 10A8 SA∅15 J3-1 7B1 TINHB

+5V R23 68 R22 68 R21 68 R20 68 CR24 CR23 CR22 CR21 CR20 CR19 CR18 CR17

INH12A J3-14 INH12B J3-13 INH13A J3-12 INH13B J3-11 INH14A J3-6 INH14B J3-5 INH15A J3-4 INH15B J3-3

SR4 SR3 SR2 SR1 T5 T4 T3 T2 CR4 CR3 CR2 CR1

C36 4700pF C35 4700pF C34 4700pF C33 4700pF R4 39 1W 1% R3 39 1W 1% R2 39 1W 1% R1 39 1W 1%

C7 .47 C123 6.8 35V 20% C8 .47 C122 6.8 35V 20% C5 .47 C6 .47 C3 .47 C121 6.8 35V 20% C4 .47 C1 .47 C2 .47

+5VI +12VI

DATA LATCHES & INHIBIT DRIVERS

SIZE	CODE IDENT NO.	3286168
D	09150	
SCALE NONE		SHEET 14 OF 15

UC-3504-08 (REV. NOV. 72) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFTG	CHK	ENGRG
D		SEE SH 1	—	—	—

3286168

SA015 GND I15B I15A I14B I14A GND SA014 SA013 GND I13B I13A I12B I12A GND SA012 SA011 GND I11B I11A I10B I10A GND SA010 SA009

I09B I09A I08B I08A GND SA008 GND GND VTH GND −5V −5V +5V +5V GND GND EBSASBX EBSASAX EBSASBX EBSASAX

GND (SA017) GND (I17B) (I17A) (I16B) (I16A) GND (SA016) SA007 GND I07B I07A I06B I06A GND SA006 SA005 GND SPARE

GND I05B I05A I04B I04A GND SA004 SA003 GND I03B I03A I02B I02A GND SA002 SA001 GND I01B I01A I00B I00A GND SA000 GND SPARE

SPARE
GND
GND
VCCH 4
VCCH 3
VCCH 2
VCCH 1
GND

GND
+5V
+5V
GND
ADR7X
ADR8X
ADR9X
GND
ADRAX
ADRBX
ADRCX
ADRDX
MADREX
MADRFX
ETM 1
ETM 2X
ETM 3X
ETM 4X
GND
SPARE

SPARE
GND
XDSCG
YDSCG
GND
VXW
VXR
GND

GND
VYW
VYR
GND
−7V
−7V
GND
IXR
IXW
GND
IYR
IYW
GND
+5V
+5V
GND
ADR3X
ADR2X
ADR1X
GND
ADR6X
ADR5X
ADR4X
GND
SPARE

ASSY 3286168-[ ]

AREA B (14)
AREA A (14)
AREA C (14)
AREA D (14)

17
3
139-934 3 PL
169-410 2 PL
SEE VIEW E ON SH 3
140-339 2 PL
140-493 3 PL

472-212
492-014
502-008
2 REQD

VIEW A-A
(TYP MTG FOR Q6 & Q8)

TABLE 1 (14)	
AREA	MAX CMPNT HT
A	.265
B	.325
C	.375
D	.525

COMPONENT SIDE

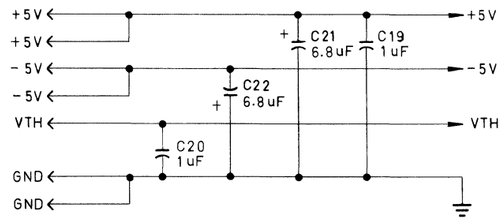
SIZE	CODE IDENT NO.	3286168
D	09150	
SCALE NONE		SHEET 15 OF 15

LIC-2286168 (REV. NOV. 78)
PRINTED IN U.S.A.

3297143

REVISIONS				
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
A		ERN 8027 (PROTOTYPE) ☆			
B		PCR 28540			
C		PCR 28572			

PART NO.	REF DESIGNATION		REMARKS
	DRIVER BOARD	SENSE AMP BOARD	
3400432-01	U1 THRU U50 U58 THRU U61		ACD
587-279	U51 THRU U56		SN74LS138
586-831	U63		SN74S04
587-280	U57		SN74S139
037-219	C21, C30.C48	C21, C22	6.8 μF
064-602	C1-C20 C22-C29 C31-C47 C49-C63		0.1 μF
064-444		C1 THRU C20	1 μF
581-403	CR1 THRU CR96	CR1 THRU CR54	
3400418-01	DM1 THRU DM6	DM7 THRU DM15	DIODE ARRAY
076-619	R1		1K, 1/4W, 2%
587-566		U82	SN74S37
3285781-01		RM1 THRU RM18	
3268257-03		U64 THRU U81	SN75234



VERSION TABLE (6)				
PART NO.	CONFIGURATION	MATS DELETED	CORE QTY	SENSE AMP BD COMPONENT NOT USED
3257067-01	32K X 16,13MIL	16, 17	524,288	U72, U73
				DM11
				RM9, RM10
				CR25 THRU CR30
				C9, C10
3257067-02	32K X 18 13MIL	———	589,824	———

(10) "0" REPRESENTS A GND LEVEL AT I/O CONNECTOR.
"1" REPRESENTS A POSITIVE LEVEL AT I/O CONNECTOR.

9. HEAVY LINE ON DIODES INDICATES CATHODE.
8. ALL RESISTOR VALUES ARE IN OHMS.
7. CAPACITOR VALUES ARE IN MFD.
(6) CONFIGURATION: TO BE PER VERSION TABLE
5. DIODE TYPE: I.C. ACD CHIP AMPEX P/N 3400432-01. OR EQUIV.
4. CORE TYPE: PER AMPEX P/N 3241352-10.
3. WIRE SIZE: X LINE — 46 AWG. Y LINE — 46 AWG. S/I LINE — 43 AWG
2. PWB TYP: DIGITIZED. FOLDED STACK.
1. WIRING: 3W-3D.

NOTES: UNLESS OTHERWISE SPECIFIED

PARTS LIST ☐

MCM8086	
3257067	32K
NEXT ASSY	USED ON
APPLICATION	

NOTICE
THIS DRAWING SHALL NOT BE DUPLICATED, USED FOR ANY PURPOSE OTHER THAN THAT FOR WHICH PROVIDED OR DISCLOSED, IN WHOLE OR IN PART, WITHOUT THE WRITTEN CONSENT OF AMPEX CORPORATION. PROVIDED, HOWEVER, THAT IF THIS DRAWING IS SPECIFIED TO BE DELIVERED TO THE GOVERNMENT, OR TO A GOVERNMENT CONTRACTOR, PURSUANT TO A GOVERNMENT PRIME OR SUBCONTRACT, THE GOVERNMENT MAY MAKE SUCH USE OF THIS DRAWING AS IS PERMITTED BY THE APPLICABLE "DATA" CLAUSE SET FORTH IN SUCH CONTRACT OR SUBCONTRACT.

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES AND INCLUDE CHEMICALLY APPLIED OR PLATED FINISHES.
TOL ± | 2 PL — | 3 PL — | ANLR —
REMOVE BURRS AND SHARP EDGES DRILL TOL PER AND 10387
INTERPRET DRAWING PER ANSI Y14.5
MATERIAL: ———
FINISH: ———

	SIGNATURE	DATE
DRAWN BY		8/27/80
CHK BY		8/28/80
DFTG APVD		
ENGRG APVD		8/27/80
AUTH BY		

AMPEX
MEMORY PRODUCTS DIVISION
200 N. Nash Street
El Segundo, California 90245

ELEC/MECH INTERFACE & SCHEMATIC

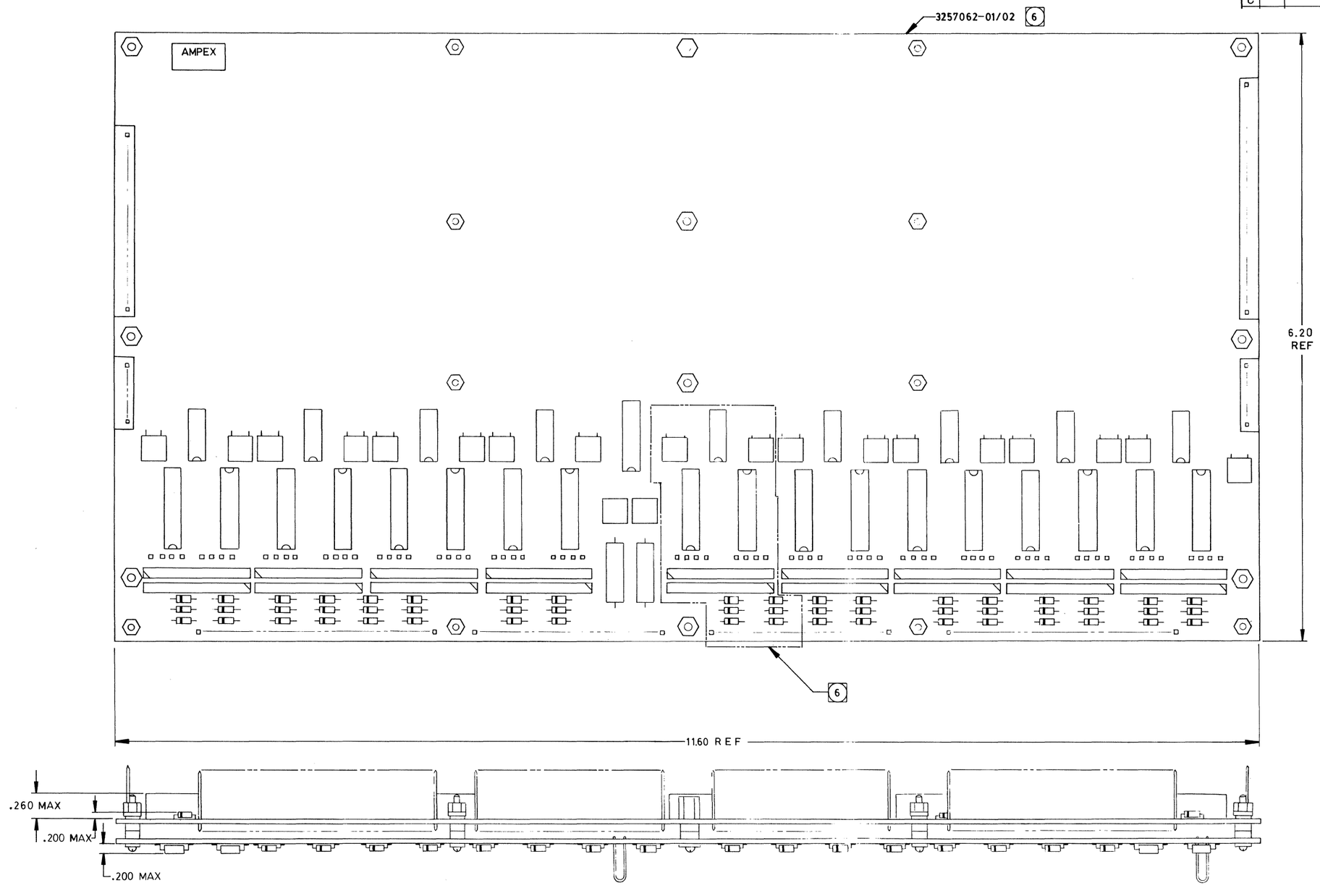
SIZE	CODE IDENT NO.	
D	09150	3297143
SCALE NONE	DO NOT SCALE THIS PRINT	SHEET 1 OF 12

AFL-PROJ

3297143

UC-2604-00 (REV. NOV. 72) PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—



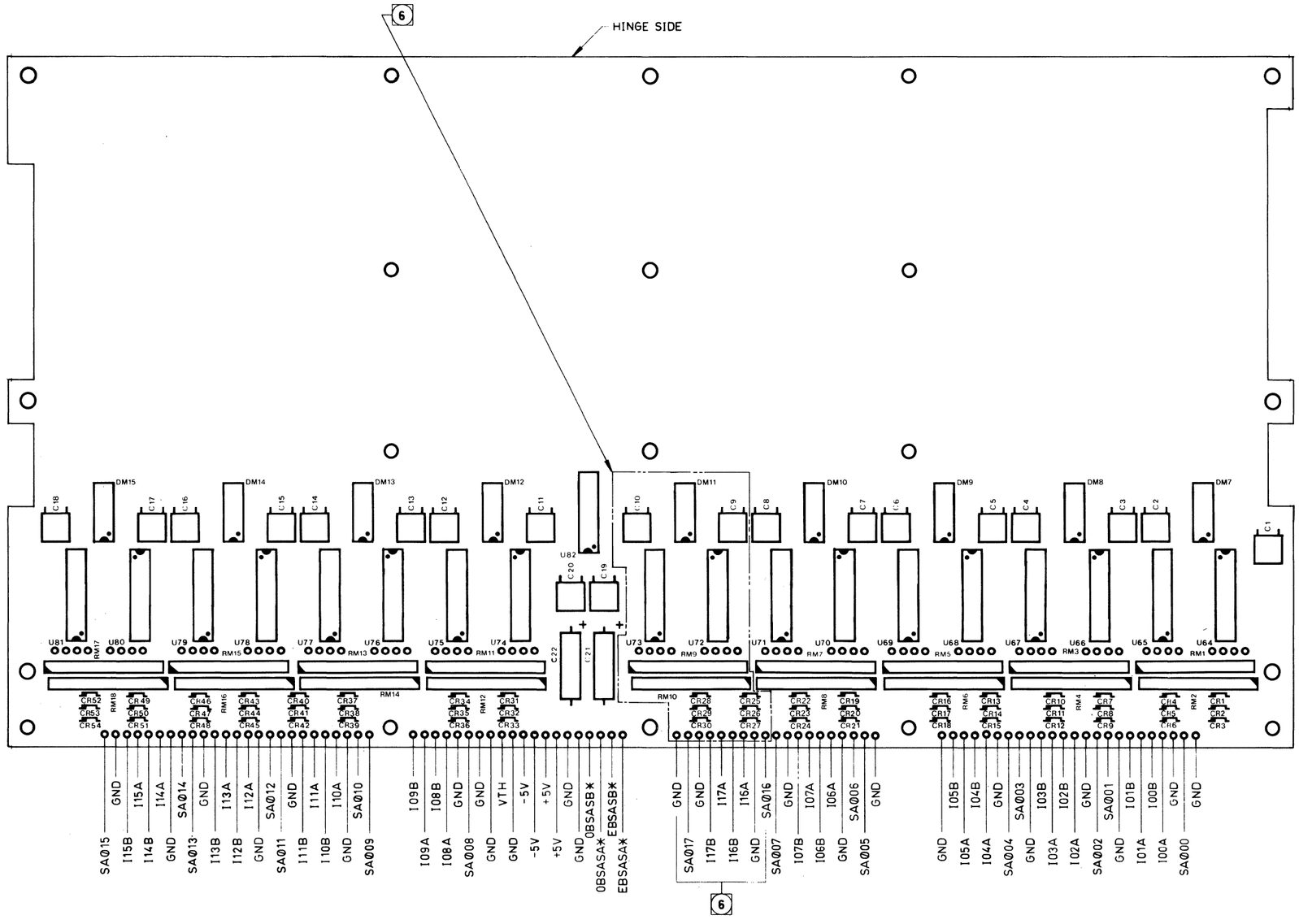
3297143

SIZE	CODE IDENT NO.	
D	09150	3 2 9 7 1 4 3
SCALE NONE		SHEET 2 OF 12

UC-3984-00 (REV. NOV. 72)
PRINTED IN U.S.A.

3297143

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—


6
HINGE SIDE
DM15 DM14 DM13 DM12 DM11 DM10 DM9 DM8 DM7
C18 C17 C16 C15 C14 C13 C12 C11 C10 C9 C8 C7 C6 C5 C4 C3 C2 C1
U82 C20 C19 C22 C21
U81 U80 U79 U78 U77 U76 U75 U74 U73 U72 U71 U70 U69 U68 U67 U66 U65 U64
RM17 RM15 RM13 RM11 RM9 RM7 RM5 RM3 RM1
RM18 RM16 RM14 RM12 RM10 RM8 RM6 RM4 RM2
CR52 CR53 CR54 CR49 CR50 CR51 CR46 CR47 CR48 CR43 CR44 CR45 CR40 CR41 CR42 CR37 CR38 CR39 CR34 CR35 CR36 CR31 CR32 CR33 CR28 CR29 CR30 CR25 CR26 CR27 CR22 CR23 CR24 CR19 CR20 CR21 CR16 CR17 CR18 CR13 CR14 CR15 CR10 CR11 CR12 CR7 CR8 CR9 CR4 CR5 CR6 CR1 CR2 CR3
GND I15A I14A SA014 GND I13A I12A GND SA012 GND I11A I10A GND SA010
SA015 I15B I14B GND SA013 I13B I12B GND SA011 I11B I10B GND SA009
I09B I08B GND GND VTH -5V +5V GND OBSASB* EBSASB*
I09A I08A SA008 GND GND -5V +5V GND OBSASA* EBSASA*
GND GND I17A I16A SA016 GND I07A I06A SA006 GND
SA017 I17B I16B GND SA007 GND I07B I06B GND SA005
GND I05B I04B GND SA003 I03B I02B GND SA001 I01B I00B GND SA000
GND I05A I04A SA004 GND I03A I02A GND SA002 GND I01A I00A GND
6

SENSE — AMP BD

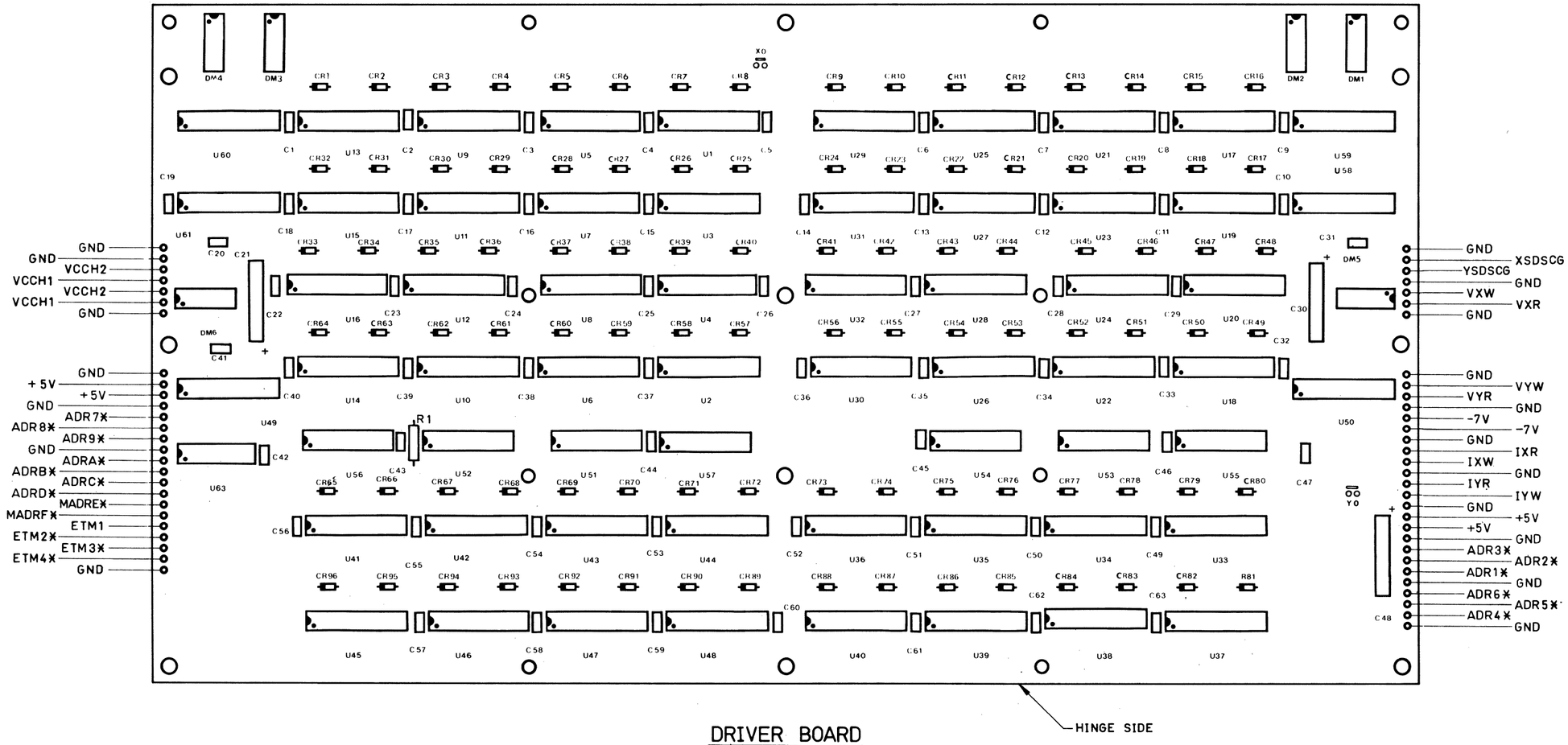
(COMPONENT SIDE)

SIZE	CODE IDENT NO.	
D	09150	3 2 9 7 1 4 3
SCALE NONE		SHEET 3 OF 12

UC-28HA-69 (REV DEC 73)
PRINTED IN U.S.A.

3297143

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—



DRIVER BOARD

(COMPONENT SIDE)

SIZE	CODE IDENT NO.	
D	09150	3 2 9 7 1 4 3
SCALE NONE		SHEET 4 OF 12

3297143

MICROFICHE UNDER PAT. NO. PRINTED IN U.S.A.

REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	——	——	——

(10) X DECODE

ADR* B	A	3	2	1		U1 / U5	U2 / U6	U3 / U7	U4 / U8	U9 / U13	U10 / U14	U11 / U15	U12 / U16	
1	1	0	0	0	XS0	0 U1-10	1 U2-10	2 U3-10	3 U4-10	64 U9-10	65 U10-10	66 U11-10	67 U12-10	U58-10 DM1-7
1	1	0	0	1	XS1	4 U1-11	5 U2-11	6 U3-11	7 U4-11	68 U9-11	69 U10-11	70 U11-11	71 U12-11	U58-11 DM1-8
1	1	0	1	0	XS2	8 U1-12	9 U2-12	10 U3-12	11 U4-12	72 U9-12	73 U10-12	74 U11-12	75 U12-12	U58-12 DM1-9
1	1	0	1	1	XS3	12 U1-15	13 U2-15	14 U3-15	15 U4-15	76 U9-15	77 U10-15	78 U11-15	79 U12-15	U58-15 DM1-10
1	1	1	0	0	XS4	16 U1-16	17 U2-16	18 U3-16	19 U4-16	80 U9-16	81 U10-16	82 U11-16	83 U12-16	U58-16 DM1-2
1	1	1	0	1	XS5	20 U1-17	21 U2-17	22 U3-17	23 U4-17	84 U9-17	85 U10-17	86 U11-17	87 U12-17	U58-17 DM1-3
1	1	1	1	0	XS6	24 U1-18	25 U2-18	26 U3-18	27 U4-18	88 U9-18	89 U10-18	90 U11-18	91 U12-18	U58-18 DM1-4
1	1	1	1	1	XS7	28 U1-9	29 U2-9	30 U3-9	31 U4-9	92 U9-9	93 U10-9	94 U11-9	95 U12-9	U58-9 DM1-5
1	0	0	0	0	XS8	32 U5-10	33 U6-10	34 U7-10	35 U8-10	96 U13-10	97 U14-10	98 U15-10	99 U16-10	U59-10 DM2-7
1	0	0	0	1	XS9	36 U5-11	37 U6-11	38 U7-11	39 U8-11	100 U13-11	101 U14-11	102 U15-11	103 U16-11	U59-11 DM2-8
1	0	0	1	0	XS10	40 U5-12	41 U6-12	42 U7-12	43 U8-12	104 U13-12	105 U14-12	106 U15-12	107 U16-12	U59-12 DM2-9
1	0	0	1	1	XS11	44 U5-15	45 U6-15	46 U7-15	47 U8-15	108 U13-15	109 U14-15	110 U15-15	111 U16-15	U59-15 DM2-10
1	0	1	0	0	XS12	48 U5-16	49 U6-16	50 U7-16	51 U8-16	112 U13-16	113 U14-16	114 U15-16	115 U16-16	U59-16 DM2-2
1	0	1	0	1	XS13	52 U5-17	53 U6-17	54 U7-17	55 U8-17	116 U13-17	117 U14-17	118 U15-17	119 U16-17	U59-17 DM2-3
1	0	1	1	0	XS14	56 U5-18	57 U6-18	58 U7-18	59 U8-18	120 U13-18	121 U14-18	122 U15-18	123 U16-18	U59-18 DM2-4
1	0	1	1	1	XS15	60 U5-9	61 U6-9	62 U7-9	63 U8-9	124 U13-9	125 U14-9	126 U15-9	127 U16-9	U59-9 DM2-5
0	1	0	0	0	XS16	128 U17-10	129 U18-10	130 U19-10	131 U20-10	192 U25-10	193 U26-10	194 U27-10	195 U28-10	U60-10 DM3-7
0	1	0	0	1	XS17	132 U17-11	133 U18-11	134 U19-11	135 U20-11	196 U25-11	197 U26-11	198 U27-11	199 U28-11	U60-11 DM3-8
0	1	0	1	0	XS18	136 U17-12	137 U18-12	138 U19-12	139 U20-12	200 U25-12	201 U26-12	202 U27-12	203 U28-12	U60-12 DM3-9
0	1	0	1	1	XS19	140 U17-15	141 U18-15	142 U19-15	143 U20-15	204 U25-15	205 U26-15	206 U27-15	207 U28-15	U60-15 DM3-10
0	1	1	0	0	XS20	144 U17-16	145 U18-16	146 U19-16	147 U20-16	208 U25-16	209 U26-16	210 U27-16	211 U28-16	U60-16 DM3-2
0	1	1	0	1	XS21	148 U17-17	149 U18-17	150 U19-17	151 U20-17	212 U25-17	213 U26-17	214 U27-17	215 U28-17	U60-17 DM3-3
0	1	1	1	0	XS22	152 U17-18	153 U18-18	154 U19-18	155 U20-18	216 U25-18	217 U26-18	218 U27-18	219 U28-18	U60-18 DM3-4
0	1	1	1	1	XS23	156 U17-9	157 U18-9	158 U19-9	159 U20-9	220 U25-9	221 U26-9	222 U27-9	223 U28-9	U60-9 DM3-5
0	0	0	0	0	XS24	160 U21-10	161 U22-10	162 U23-10	163 U24-10	224 U29-10	225 U30-10	226 U31-10	227 U32-10	U61-10 DM4-7
0	0	0	0	1	XS25	164 U21-11	165 U22-11	166 U23-11	167 U24-11	228 U29-11	229 U30-11	230 U31-11	231 U32-11	U61-11 DM4-8
0	0	0	1	0	XS26	168 U21-12	169 U22-12	170 U23-12	171 U24-12	232 U29-12	233 U30-12	234 U31-12	235 U32-12	U61-12 DM4-9
0	0	0	1	1	XS27	172 U21-15	173 U22-15	174 U23-15	175 U24-15	236 U29-15	237 U30-15	238 U31-15	239 U32-15	U61-15 DM4-10
0	0	1	0	0	XS28	176 U21-16	177 U22-16	178 U23-16	179 U24-16	240 U29-16	241 U30-16	242 U31-16	243 U32-16	U61-16 DM4-2
0	0	1	0	1	XS29	180 U21-17	181 U22-17	182 U23-17	183 U24-17	244 U29-17	245 U30-17	246 U31-17	247 U32-17	U61-17 DM4-3
0	0	1	1	0	XS30	184 U21-18	185 U22-18	186 U23-18	187 U24-18	248 U29-18	249 U30-18	250 U31-18	251 U32-18	U61-18 DM4-4
0	0	1	1	1	XS31	188 U21-9	189 U22-9	190 U23-9	191 U24-9	252 U29-9	253 U30-9	254 U31-9	255 U32-9	U61-9 DM4-5

		U17 / U21	U18 / U22	U19 / U23	U20 / U24	U25 / U29	U26 / U30	U27 / U31	U28 / U32
ADR*	9	0	0	0	0	1	1	1	1
	8	0	0	1	1	0	0	1	1
	7	0	1	0	1	0	1	0	1

(10) Y DECODE

	U33 / U41	U34 / U42	U35 / U43	U36 / U44	U37 / U45	U38 / U46	U39 / U47	U40 / U48		ADR* F	6	5	4
YS0	0 U33-10	1 U34-10	4 U35-10	5 U36-10	64 U37-10	65 U38-10	68 U39-10	69 U40-10	U49-10 DM6-7	1	0	0	0
YS1	8 U33-11	9 U34-11	12 U35-11	13 U36-11	72 U37-11	73 U38-11	76 U39-11	77 U40-11	U49-11 DM6-8	1	0	0	1
YS2	16 U33-12	17 U34-12	20 U35-12	21 U36-12	80 U37-12	81 U38-12	84 U39-12	85 U40-12	U49-12 DM6-9	1	0	1	0
YS3	24 U33-15	25 U34-15	28 U35-15	29 U36-15	88 U37-15	89 U38-15	92 U39-15	93 U40-15	U49-15 DM6-10	1	0	1	1
YS4	32 U33-16	33 U34-16	36 U35-16	37 U36-16	96 U37-16	97 U38-16	100 U39-16	101 U40-16	U49-16 DM6-2	1	1	0	0
YS5	40 U33-17	41 U34-17	44 U35-17	45 U36-17	104 U37-17	105 U38-17	108 U39-17	109 U40-17	U49-17 DM6-3	1	1	0	1
YS6	48 U33-18	49 U34-18	52 U35-18	53 U36-18	112 U37-18	113 U38-18	116 U39-18	117 U40-18	U49-18 DM6-4	1	1	1	0
YS7	56 U33-9	57 U34-9	60 U35-9	61 U36-9	120 U37-9	121 U38-9	124 U39-9	125 U40-9	U49-9 DM6-5	1	1	1	1
YS8	2 U41-10	3 U42-10	6 U43-10	7 U44-10	66 U45-10	67 U46-10	70 U47-10	71 U48-10	U50-10 DM5-5	0	0	0	0
YS9	10 U41-11	11 U42-11	14 U43-11	15 U44-11	74 U45-11	75 U46-11	78 U47-11	79 U48-11	U50-11 DM5-4	0	0	0	1
YS10	18 U41-12	19 U42-12	22 U43-12	23 U44-12	82 U45-12	83 U46-12	86 U47-12	87 U48-12	U50-12 DM5-3	0	0	1	0
YS11	26 U41-15	27 U42-15	30 U43-15	31 U44-15	90 U45-15	91 U46-15	94 U47-15	95 U48-15	U50-15 DM5-2	0	0	1	1
YS12	34 U41-16	35 U42-16	38 U43-16	39 U44-16	98 U45-16	99 U46-16	102 U47-16	103 U48-16	U50-16 DM5-10	0	1	0	0
YS13	42 U41-17	43 U42-17	46 U43-17	47 U44-17	106 U45-17	107 U46-17	110 U47-17	111 U48-17	U50-17 DM5-9	0	1	0	1
YS14	50 U41-18	51 U42-18	54 U43-18	55 U44-18	114 U45-18	115 U46-18	118 U47-18	119 U48-18	U50-18 DM5-8	0	1	1	0
YS15	58 U41-9	59 U42-9	62 U43-9	63 U44-9	122 U45-9	123 U46-9	126 U47-9	127 U48-9	U50-9 DM5-7	0	1	1	1

ADR*	E	0	0	0	0	1	1	1	1
	D	0	0	1	1	0	0	1	1
	C	0	1	0	1	0	1	0	1

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REVISIONS					
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C		SEE SH 1	—	—	—

WORST CASE PATTERN

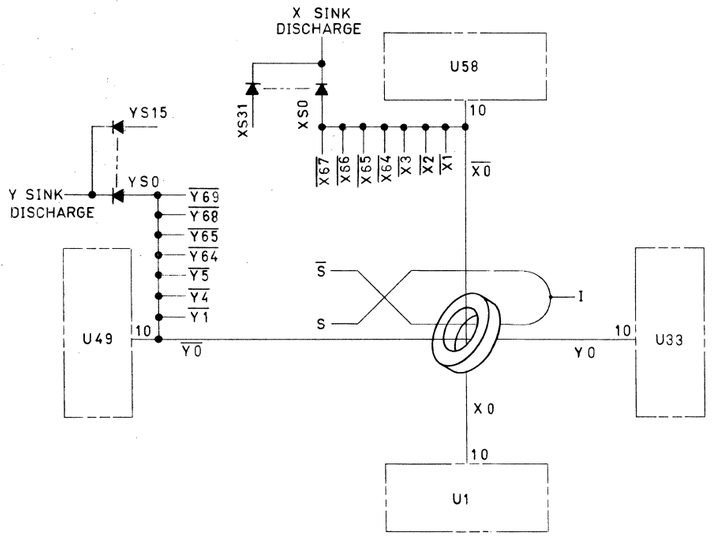
	Y0	Y1	Y2	Y3	Y124	Y125	Y126	Y127
X0	1	0	1	0	1	0	1	0
X1	1	0	1	0	1	0	1	0
X2	1	0	1	0	1	0	1	0
X127	1	0	1	0	1	0	1	0
X128	0	1	0	1	0	1	0	1
X129	0	1	0	1	0	1	0	1
X255	0	1	0	1	0	1	0	1

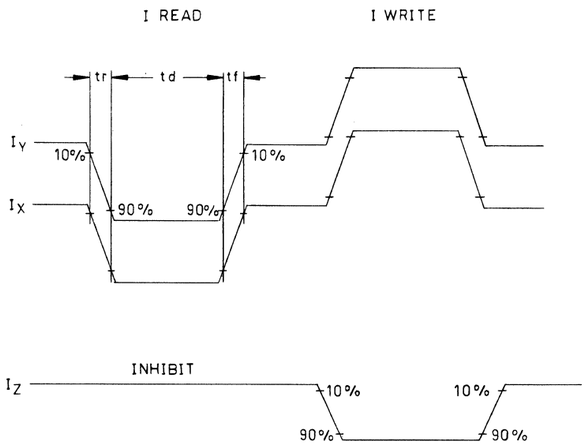
LINE RESISTANCE (K)

LINE RESISTANCE AT 25°C	13 MIL CORE STACK MIN	NOM	MAX
X LINE			
Y LINE			
SENSE/INHIBIT (HALF)			

LINE INDUCTANCE (K)

LINE INDUCTANCE	13 MIL CORE STACK
X LINE	
Y LINE	
INHIBIT EACH HALF TWO HALVES IN PARALLEL	





STACK PERFORMANCE

td = NS		tr = NS	
MIN ONE @ tp (MV)	tp ± 15 NSC	MAX dvz (MV) @ tp OF ONE	ts MAX NSC

TYP OPERATING CONDITIONS AT +25 °C

CURRENT AMPLITUDES (MA) ± 1%				
READ		WRITE		INHIBIT DIGIT
X	Y	X	Y	

TYPICAL TEST PROGRAM TIMING

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1			

8D8 IXW
8D8 IXR
8C8 ADR1*
8C8 ADR2*
8B8 ADR3*
8D8 VCCH1

U1 ACD: CR7, CR8; U51-15; X00 X04 X08 X12 X16 X20 X24 X28
U2 ACD: CR58, CR57; U51-14; X01 X05 X09 X13 X17 X21 X25 X29
U3 ACD: CR26, CR25; U51-13; X02 X06 X10 X14 X18 X22 X26 X30
U4 ACD: CR39, CR40; U51-12; X03 X07 X11 X15 X19 X23 X27 X31
U5 ACD: CR5, CR6; U52-15; X32 X36 X40 X44 X48 X52 X56 X60
U6 ACD: CR60, CR59; U52-14; X33 X37 X41 X45 X49 X53 X57 X61
U7 ACD: CR28, CR27; U52-13; X34 X38 X42 X46 X50 X54 X58 X62
U8 ACD: CR37, CR38; U52-12; X35 X39 X43 X47 X51 X55 X59 X63
U9 ACD: CR3, CR4; U51-11; X64 X68 X72 X76 X80 X84 X88 X92
U10 ACD: CR62, CR61; U51-10; X65 X69 X73 X77 X81 X85 X89 X93
U11 ACD: CR30, CR29; U51-9; X66 X70 X74 X78 X82 X86 X90 X94
U12 ACD: CR35, CR36; U51-7; X67 X71 X75 X79 X83 X87 X91 X95
U13 ACD: CR1, CR2; U52-11; X96 X100 X104 X108 X112 X116 X120 X124
U14 ACD: CR64, CR63; U52-10; X97 X101 X105 X109 X113 X117 X121 X125
U15 ACD: CR32, CR31; U52-9; X98 X102 X106 X110 X114 X118 X122 X126
U16 ACD: CR33, CR34; U52-7; X99 X103 X107 X111 X115 X119 X123 X127

+5V, -7V

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE		
			DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—

IXW
IXR
VCCH1
ADR1
ADR2
ADR3

U17 ACD — CR15, CR16 — U53-15 — X128 X132 X136 X140 X144 X148 X152 X156
U18 ACD — CR50, CR49 — U53-14 — X129 X133 X137 X141 X145 X149 X153 X157
U19 ACD — CR18, CR17 — U53-13 — X130 X134 X138 X142 X146 X150 X154 X158
U20 ACD — CR47, CR48 — U53-12 — X131 X135 X139 X143 X147 X151 X155 X159
U21 ACD — CR13, CR14 — U54-15 — X160 X164 X168 X172 X176 X180 X184 X188
U22 ACD — CR52, CR51 — U54-14 — X161 X165 X169 X173 X177 X181 X185 X189
U23 ACD — CR20, CR19 — U54-13 — X162 X166 X170 X174 X178 X182 X186 X190
U24 ACD — CR45, CR46 — U54-12 — X163 X167 X171 X175 X179 X183 X187 X191
U25 ACD — CR11, CR12 — U53-11 — X192 X196 X200 X204 X208 X212 X216 X220
U26 ACD — CR54, CR53 — U53-10 — X193 X197 X201 X205 X209 X213 X217 X221
U27 ACD — CR22, CR21 — U53-9 — X194 X198 X202 X206 X210 X214 X218 X222
U28 ACD — CR43, CR44 — U53-7 — X195 X199 X203 X207 X211 X215 X219 X223
U29 ACD — CR9, CR10 — U54-11 — X224 X228 X232 X236 X240 X244 X248 X252
U30 ACD — CR56, CR55 — U54-10 — X225 X229 X233 X237 X241 X245 X249 X253
U31 ACD — CR24, CR23 — U54-9 — X226 X230 X234 X238 X242 X246 X250 X254
U32 ACD — CR41, CR42 — U54-7 — X227 X231 X235 X239 X243 X247 X251 X255

+5V, −7V, VCCH, VEE

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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—

IYW
IYR
ADR4*
ADR5*
ADR6*
VCCH1

U33 ACD — CR79, CR80 — U55-15
U34 ACD — CR77, CR78 — U55-14
U35 ACD — CR75, CR76 — U55-13
U36 ACD — CR73, CR74 — U55-12
U37 ACD — CR82, CR81 — U55-11
U38 ACD — CR84, CR83 — U55-10
U39 ACD — CR86, CR85 — U55-9
U40 ACD — CR88, CR87 — U55-7
U41 ACD — CR65, CR66 — U56-15
U42 ACD — CR67, CR68 — U56-14
U43 ACD — CR69, CR70 — U56-13
U44 ACD — CR71, CR72 — U56-12
U45 ACD — CR96, CR95 — U56-11
U46 ACD — CR94, CR93 — U56-10
U47 ACD — CR92, CR91 — U56-9
U48 ACD — CR90, CR89 — U56-7

Each: +5V, −7V, VCCH, VEE, VW, VR, A0, A1, A2, Ē, 00–07

U33: Y00 Y08 Y16 Y24 Y32 Y40 Y48 Y56
U34: Y01 Y09 Y17 Y25 Y33 Y41 Y49 Y57
U35: Y04 Y12 Y20 Y28 Y36 Y44 Y52 Y60
U36: Y05 Y13 Y21 Y29 Y37 Y45 Y53 Y61
U37: Y64 Y72 Y80 Y88 Y96 Y104 Y112 Y120
U38: Y65 Y73 Y81 Y89 Y97 Y105 Y113 Y121
U39: Y68 Y76 Y84 Y92 Y100 Y108 Y116 Y124
U40: Y69 Y77 Y85 Y93 Y101 Y109 Y117 Y125
U41: Y02 Y10 Y18 Y26 Y34 Y42 Y50 Y58
U42: Y03 Y11 Y19 Y27 Y35 Y43 Y51 Y59
U43: Y06 Y14 Y22 Y30 Y38 Y46 Y54 Y62
U44: Y07 Y15 Y23 Y31 Y39 Y47 Y55 Y63
U45: Y66 Y74 Y82 Y90 Y98 Y106 Y114 Y122
U46: Y67 Y75 Y83 Y91 Y99 Y107 Y115 Y123
U47: Y70 Y78 Y86 Y94 Y102 Y110 Y118 Y126
U48: Y71 Y79 Y87 Y95 Y103 Y111 Y119 Y127

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SIZE	CODE IDENT NO.	
D	09150	3 2 9 7 1 4 3
SCALE NONE		SHEET 9 OF 12

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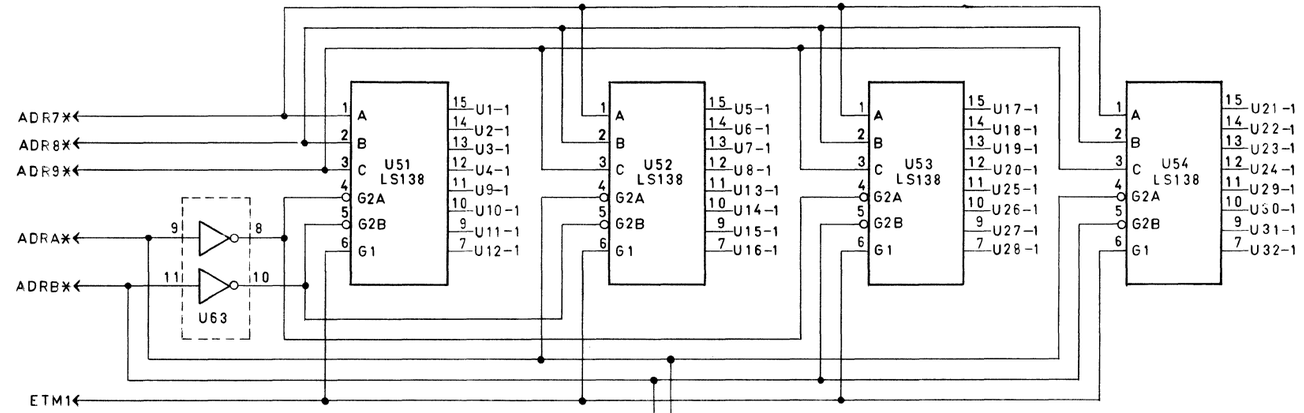
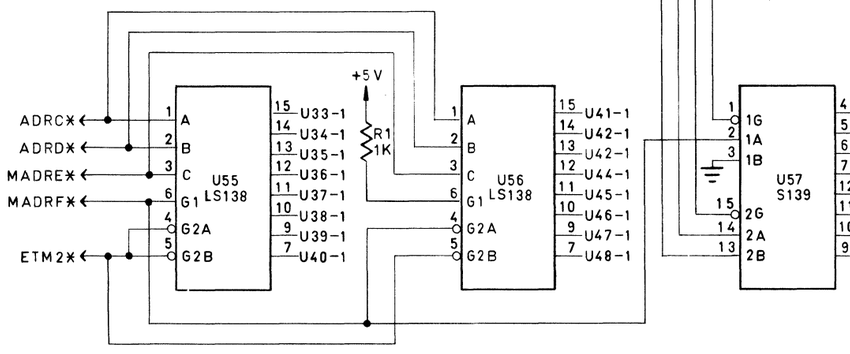
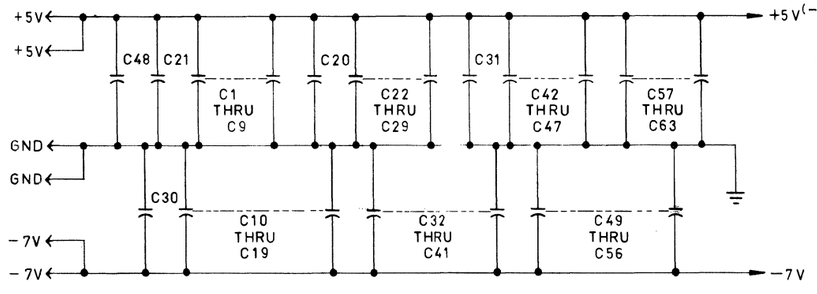
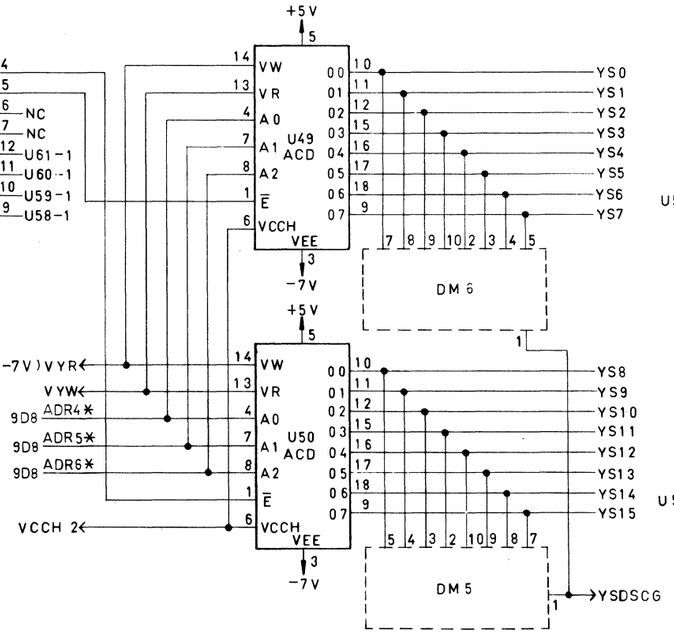
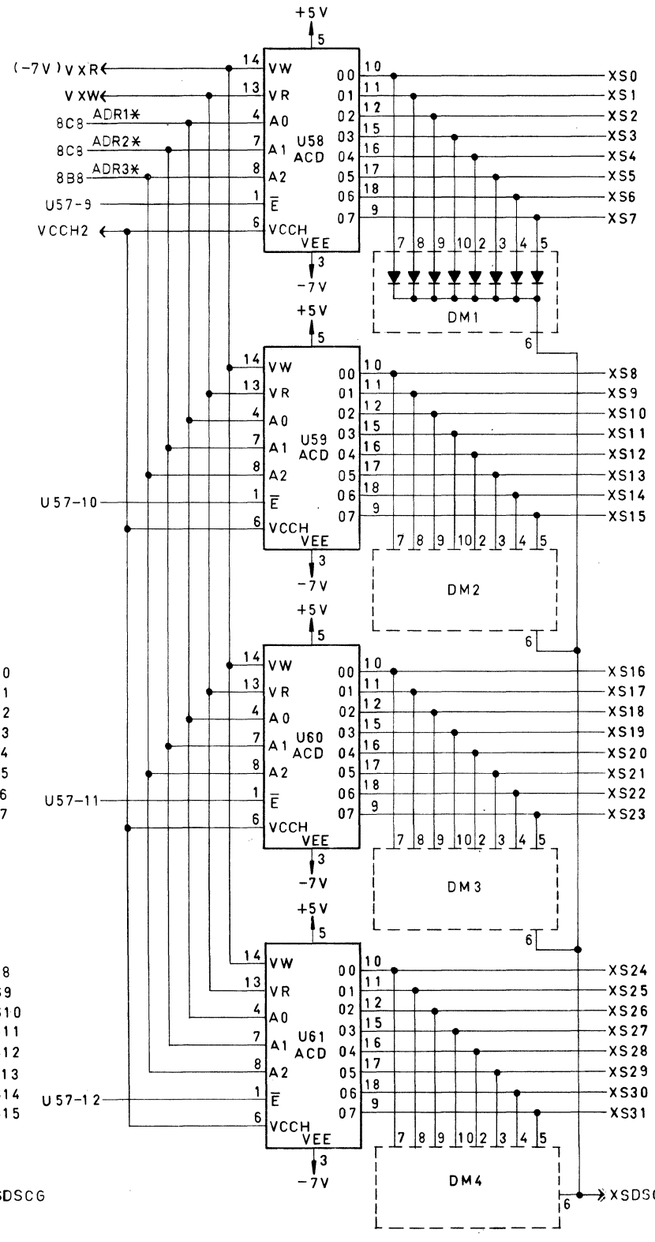
REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1	—	—	—











SIZE	CODE IDENT NO.	
D	09150	3297143
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REVISIONS					
LTR	ZONE	DESCRIPTION	SIGNATURE AND DATE DFTG	CHK	ENGRG
C		SEE SH 1			

VTH
RM4
-5V+5V
C3
S02A
S02A
I02A
CR8
DM8
S02B
S02B
I02B
CR7
CR9
U66
75234
SA002
U82
S37
EBSASB*
RM1
+5V-5V
C2
S01A
S01A
I01A
CR5
DM7
S01B
S01B
I01B
CR4
CR6
U65
75234
SA001
RM2
-5V+5V
C1
S00A
S00A
I00A
CR2
DM7
S00B
S00B
I00B
CR1
CR3
U64
75234
SA000
RM5
+5V-5V
C6
S05B
S05B
I05B
CR17
DM9
S05A
S05A
I05A
CR16
CR18
U69
75234
SA005
U82
S37
EBSASA*
RM6
-5V+5V
C5
S04B
S04B
I04B
CR14
DM9
S04A
S04A
I04A
CR13
CR15
U68
75234
SA004
RM3
+5V-5V
C4
S03B
S03B
I03B
CR10
DM8
S03A
S03A
I03A
CR11
CR12
U67
75234
SA003
RM10
-5V+5V
C9
S16A
S16A
I16A
CR25
DM11
S16B
S16B
I16B
CR26
CR27
U72
75234
SA016
6
RM7
+5V-5V
C8
S07A
S07A
I07A
CR22
DM10
S07B
S07B
I07B
CR23
CR24
U71
75234
SA007
RM8
-5V+5V
C7
S06A
S06A
I06A
CR20
DM10
S06B
S06B
I06B
CR19
CR21
U70
75234
SA006

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D	09150	3297143
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REVISIONS					
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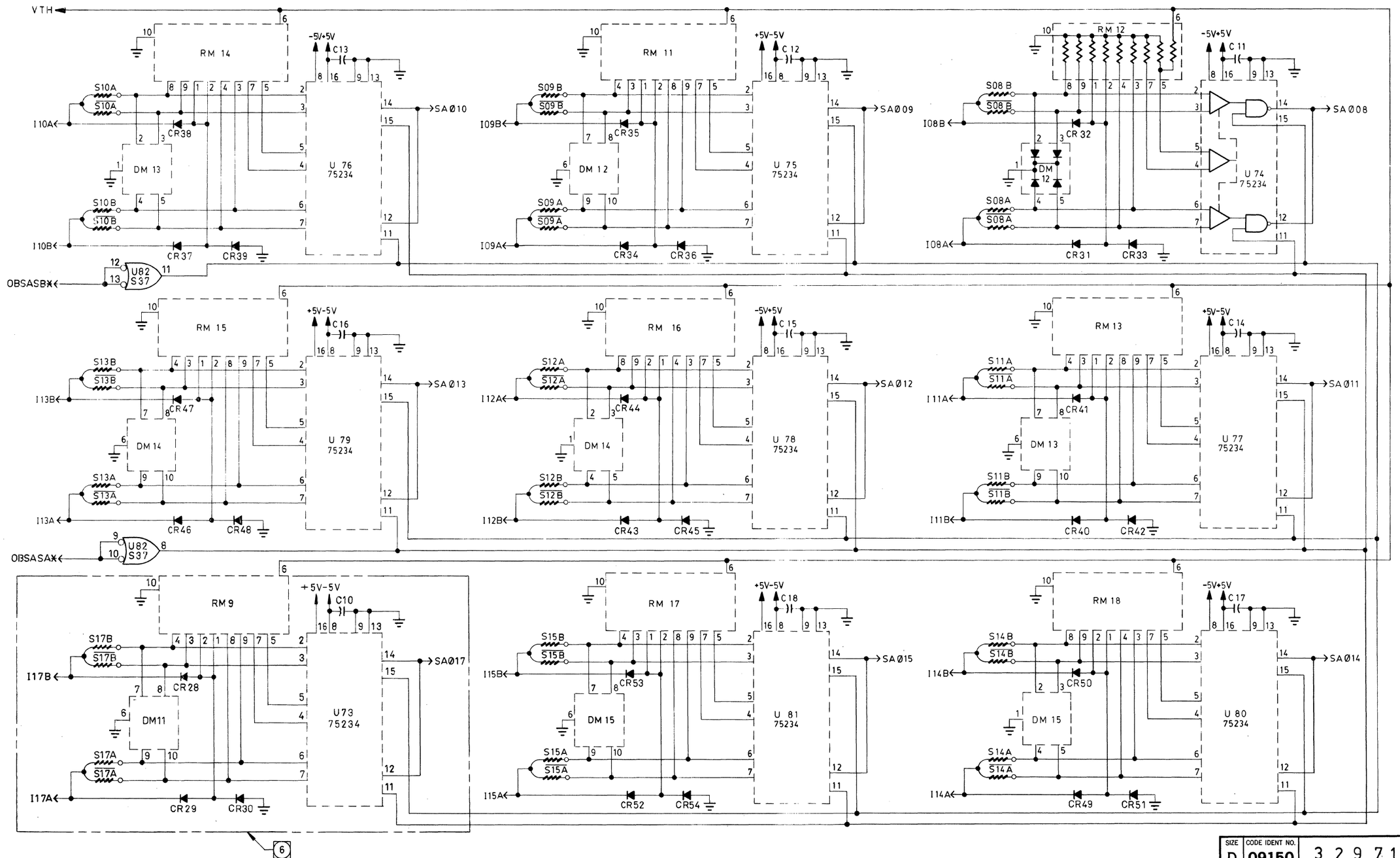
C		SEE SHT 1	—	—	—



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SIZE	CODE IDENT NO.	
D	09150	3 2 9 7 1 4 3
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SECTION IV
MAINTENANCE PROCEDURES

4.1 GENERAL

This section contains maintenance instructions for the MCM-8086 Microcomputer Core Memory module. A recommended preventive maintenance schedule is included, and related maintenance procedures are provided.

4.2 TOOLS AND TEST EQUIPMENT

A list of tools and test equipment (or equivalent) required for maintenance operations is provided in Table 4-1. Observe standard electronic maintenance practices when checking and/or replacing system components. Only persons experienced in using the equipment should perform maintenance procedures.

Table 4-1. Tools and Test Equipment Required

Test Equipment	Vendor	Model/ Part No.
Oscilloscope	Tektronix	Type 585
Dual-Trace Amplifier	Tektronix	Type CA
Differential Preamplifier	Tektronix	Type W
Multimeter	Simpson	Type 260
Alligator Clips	Mueller	No. 30
Insulators	Mueller	No. 32
Common Hand Tools		

4.3 PREVENTIVE MAINTENANCE

The MCM-8086 memory modules require minimal maintenance because of the all-electronic nature of the equipment. However, a preventive maintenance program consisting of electrical checks is recommended as an aid in obtaining maximum operating efficiency from the system. A schedule of recommended maintenance procedures is shown in Table 4-2. Subsequent paragraphs describe the procedures listed in the table.

4.3.1 Dc Operating Voltages

The dc operating voltages provided by the system power supply should be checked weekly to verify that voltage levels are within allowable limits. These limits are specified in Table 4-3. If the limits are exceeded, make the necessary adjustments to return the operating voltage to its nominal level. Minor changes in voltage levels may be corrected by adjusting the dc output of the system power supply.

Table 4-2. Preventive Maintenance Schedule

Time Interval			Maintenance Operation
Weekly	Monthly	Semi-Annually	
X	X	X	Operating Voltage Checks
		X	Visual Inspection of PWBAs
		X	Visual Inspection of Power Supply

The procedures for checking the dc operating voltages depend on system configuration. However, all voltages should be checked using a multimeter, and all measurements should be referenced to the circuit ground (memory module I/O connector pins 1, 2, 11, 12, 85, 86). Refer to the appropriate system manual for detailed instructions.

Table 4-3. Dc Operating Voltages

Circuit	Connector Pin	Voltage Level
+5 VDC	Component Side: 3, 5, 81, 83 Dip Side: 4, 6, 82, 84	+4.75V to +5.25V
+12 VDC	7 Component, 8 Dip	+11.4V to 12.6V

4.3.2 Worst Pattern and System Operational Checks

Worst pattern and system operational checks test the memory modules for accurate data retrieval in the presence of deliberately generated "delta noise." The sense/inhibit winding links the cores of a matrix so that

maximum cancellation of disturb noise occurs at the output of the sense winding. However, if the noise produced by the half-select currents through cores in the ZERO state is not exactly equal to that produced by the half-select currents through the cores in the ONE state, cancellation is less than perfect and an accumulative noise signal, called delta noise, appears at the output of that sense line. Thus, if all cores that produce negative signals at the output terminals of a sense/inhibit winding contain ONEs and all others contain ZEROs, the maximum delta noise is produced on that sense/inhibit winding when reading from any address. The data pattern that deliberately induces maximum delta noise is called a worst case delta noise pattern or, simply, worst pattern.

The worst pattern logic that relates address and data content for writing the pattern into the memory is:

$$\text{WP Data} = \text{ADD11} \oplus \text{ADD12}$$

Worst pattern checks should be performed in conjunction with a subsequent system operational check. The checks may be accomplished through CPU or memory tester programming. To perform the checks, proceed as follows:

1. Check all power supply voltages.
2. Write worst pattern into memory at all addresses.
3. Operate memory unit for a period of 30 seconds in read-restore mode.
4. Cycle memory through all addresses and:
   a. Perform read-restore operation at each address.
   b. Check for errors in worst pattern readout at each address.
5. Record addresses at which any errors occur and numbers of data bits which failed.

NOTE

If errors occur, continue the address cycling and error checking operations. In the event of repetitive errors, refer to the corrective maintenance procedures included in this section.

4.3.3 Semiannual Maintenance Check

The purpose of the semiannual maintenance check is to verify the general operational status and condition of the memory unit. In addition to performing the weekly and monthly checks previously described, the semiannual check includes the following visual inspection of the memory unit.

CAUTION

When removing a core memory module from the mulitple memory system or when disconnecting a plug or connector, turn off dc power. Removing or inserting core memory modules while the power is on may damage the equipment. Ensure that all printed circuit boards and connectors make proper contact in their sockets.

Inspect the core memory module for evidence of overheated components, excessive dirt or foreign material, or physical damage. Inspect PWBA connectors for dust, corrosion, or foreign material; vacuum clean if dirty.

NOTE

If any of the components show evidence of overheating, replace or repair the PWBA to prevent possible failure during a data processing operation.

4.4 CORRECTIVE MAINTENANCE

Corrective maintenance procedures include memory system checks which are not part of the preventive maintenance activities. PWBA replacement usually corrects operational discrepancies.

NOTE

The MCM-8086 memory module contains no user operating adjustments. Repairs should be limited to replacement of complete assemblies. Component repairs should be made only by persons familiar with the equipment and with electronic repair techniques.

4.4.1 Troubleshooting

Ampex recommends a functional analysis approach to locate the source of a problem. (The principles of system operation and circuit functions presented in Section III of this manual provides a foundation for troubleshooting the system.) Use the timing charts in Section III and logic diagrams in Appendix A during analysis and troubleshooting.

To provide a systematic approach to fault analysis and identification, it is recommended that corrective maintenance actions be conducted in the following sequence:

1. Visually inspect equipment for loose connections, damage, etc., by verifying the integrity of the interface connections and the physical condition of the equipment.

2. Ensure that the PWBAs are correctly installed in the appropriate slots in the chassis.

3. Check external power supply operation and voltages.

4. Check related circuits on memory board.

5. Perform system functional checks.

4.4.2 System Checks

Memory system problems may be categorized as follows:

1. Malfunctions caused by faulty reference control, input logic, and timing.

2. Partial data word failures caused by faulty drive and sink switches, drive control, data register, inhibit drive state, stack decoding, or line drive circuits.

3. Address failures caused by faulty address decoder.

In addition to performing multimodule system operational tests to localize and identify the cause of a problem, it is recommended that identical PWBA modules be interchanged during the course of the tests. By so doing, it may be possible to trace a fault to a particular PWBA by noting a shift in the faulty bits in addresses. Verify such a condition, or similar conditions in which a PWBA is suspect, by replacing the suspect board with a spare PWBA of the same type, and note whether so doing eliminates the fault condition.

After power supply operation and voltages have been verified as being correct, conduct the following tests to localize a malfunction in the memory system:

1. Initiate a memory operation at each address and check each readout data word.

2. Check results for:

   a. Mulfunctions in which there is no apparent response to commands applied to memory, or in which identical readout data words occur at each address.

   b. Partial data word failures in which failure of one bit, or a series of bits, occurs at all addresses.

   c. Address failures in which faulty memory operation occurs at a particular address only.

4.4.2.1 Localizing System Malfunctions

If power input voltages are normal and malfunction condition persists, check the operating voltages and signals at the PWBA connector pins.

4.4.2.2. Locating Drive Circuit Malfunctions

Reading data from or writing data into the magnetics depends upon proper operation of the read or write sink switch, the drive switch, and the drive control circuit selected by decoding a portion of the address. Failure to read or write at a selected address indicates a possible malfunction of one or more switches.

4.4.2.3 Locating Core Matrix Malfunctions

Problems within the magnetic core matrices are unlikely under normal operating conditions. However, continuity measurements of the core winding enable maintenance personnel to check the module wiring.

CAUTION

The matrices and connectors may be damaged by improper test procedures. Do not probe matrix windings. Apply test probes only to the printed circuit etch.

4.4.2.4 Locating Sense/Inhibit Malfunctions

Failure of a particular sense circuit results in the register for the corresponding bit indicating a ZERO at each and every address. Failure of a particular inhibit circuit results in the register for the corresponding bit indicating a ONE at each and every address. If operational

checks indicate no inputs to a sense/inhibit circuit, make continuity checks for the open sense/inhibit line.

4.5 REPAIRS

For repairs other than minor faults such as a broken lead or solder joint, remove and replace the item as an assembly. Assemblies may then be returned to the factory for rework. In any event, repairs involving checking and/or replacement of discrete components should be performed by experienced personnel only.

APPENDIX A
REFERENCE DRAWINGS

This section contains pertinent drawings and a mnemonic listing for the Ampex MCM-8086 Microcomputer Core Memory module, as listed below.

Title	Dwg No.
Mnemonic Listing	-----
Memory Module Assembly	3286074
Timing & Control Board	3286075
Timing & Control Board	3286149
Elec/Mech Interface & Schematic	3297143

Mnemonic Listing

Mnemonic	Definition
ADR	Address
ADRE, ADRF	Module Select Address
BHEN	Byte High Enable
DAT	Data Input/Output
INH	Inhibit Memory
INIT	Initialization
MRDC	Memory Read Command
MWTC	Memory Write Command
XACK	Transfer Acknowledge

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